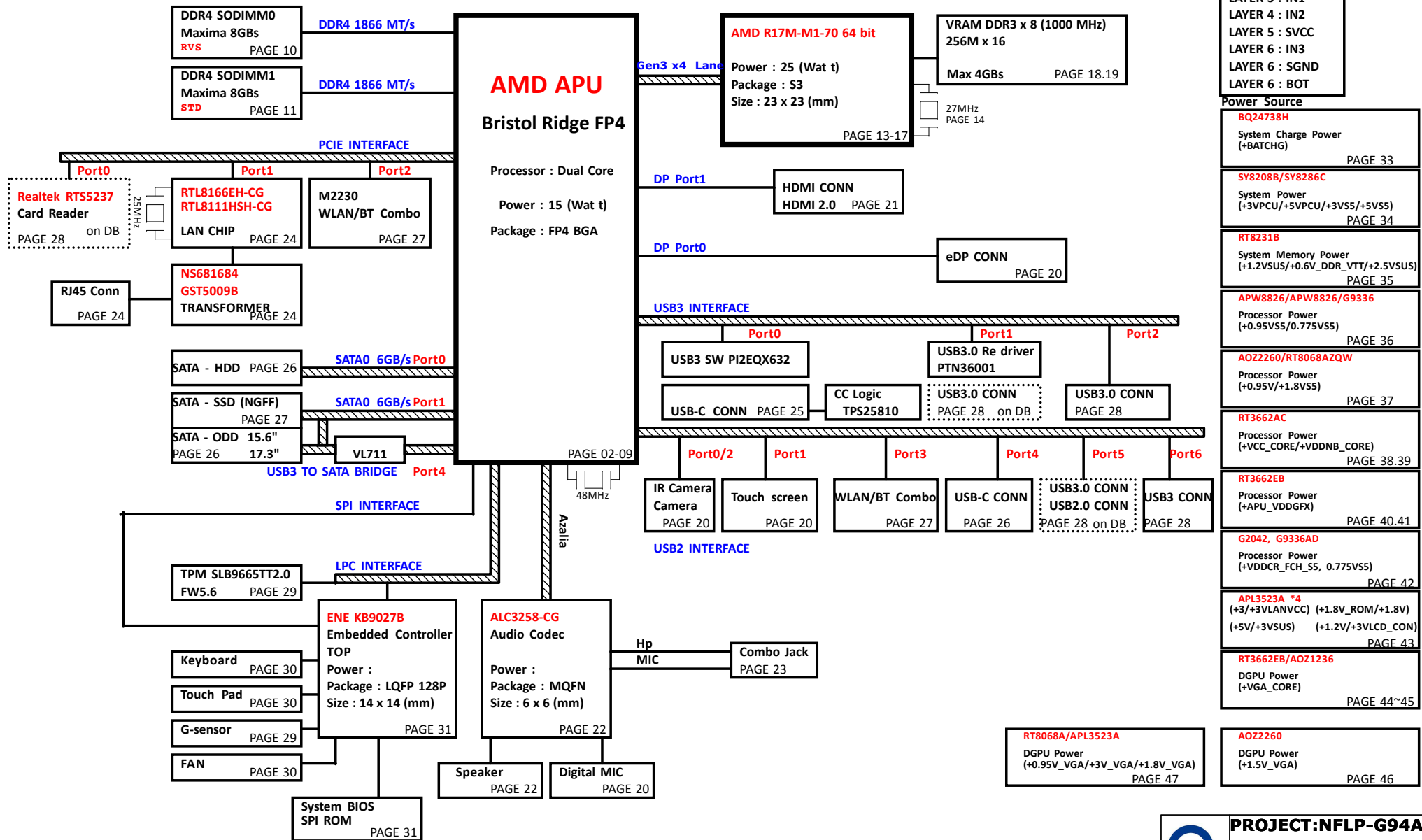


G94A 15.6"/17.3" 2SPD System Block Diagram-AMD Bristol FP4 01




PCB 8L STACK UP

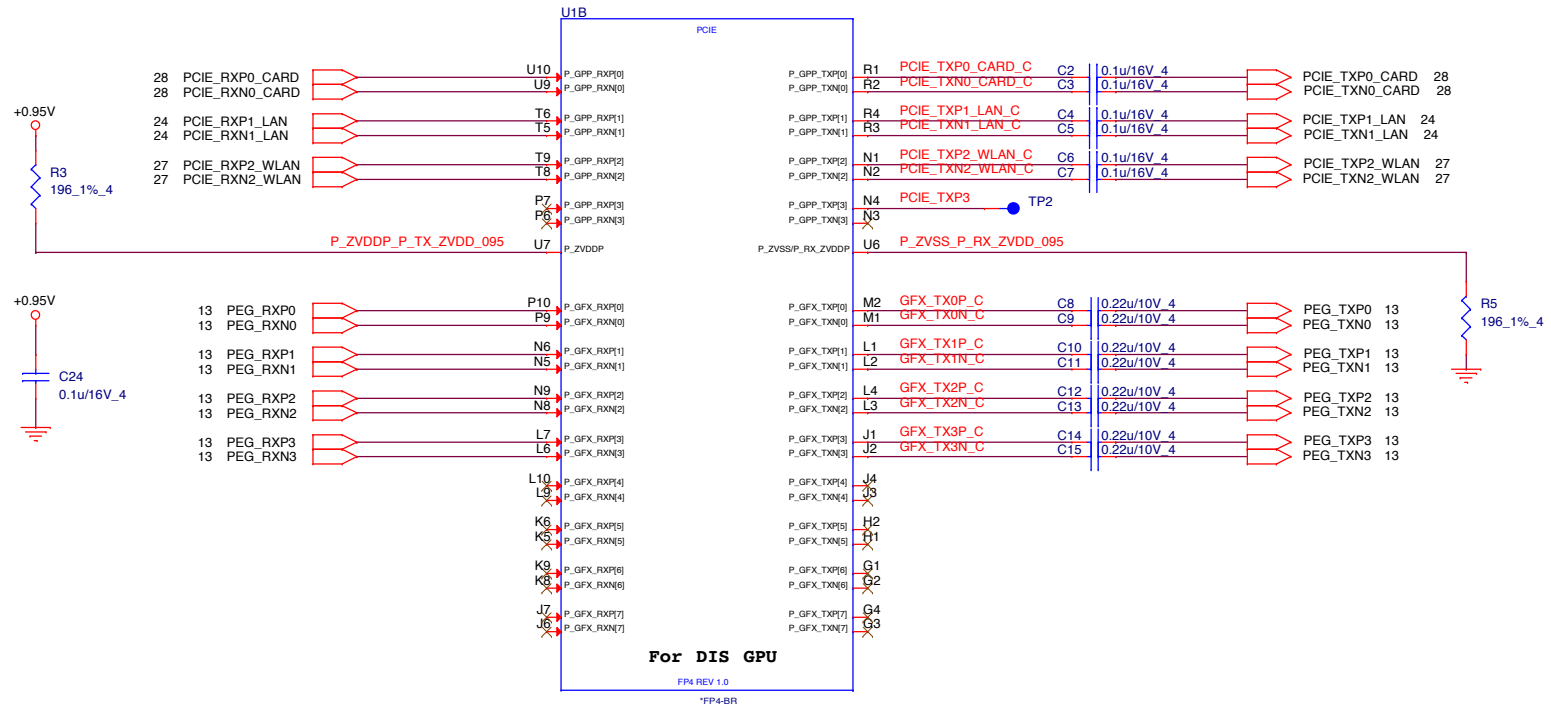
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 6 : SGND
LAYER 6 : BOT

Power Source

BQ24738H System Charge Power (+BATCHG) PAGE 33
SY8208B/SY8286C System Power (+3VPCU/+5VPCU/+3VSS/+5VSS) PAGE 34
RT8231B System Memory Power (+1.2VSUS/+0.6V_DDR_VTT/+2.5VSUS) PAGE 35
APW8826/APW8826/G9336 Processor Power (+0.95V5/0.775V55) PAGE 36
AO22260/RT8068AZQW Processor Power (+0.95V/+1.8V55) PAGE 37
RT3662AC Processor Power (+VCC_CORE/+VDDNB_CORE) PAGE 38.39
RT3662EB Processor Power (+APU_VDDGFX) PAGE 40.41
G2042, G9336AD Processor Power (+VDDCR_FCH_S5, 0.775V55) PAGE 42
APL3523A *4 (+3/+3VLAVCC) (+1.8V_ROM/+1.8V) (+5V/+3VSUS) (+1.2V/+3VLCD_CON) PAGE 43
RT3662EB/AO21236 DGPU Power (+VGA_CORE) PAGE 44~45
RT8068A/APL3523A DGPU Power (+0.95V_VGA/+3V_VGA/+1.8V_VGA) PAGE 47
AO22260 DGPU Power (+1.5V_VGA) PAGE 46

**PROJECT:NFLP-G94A**
Quanta Computer Inc.

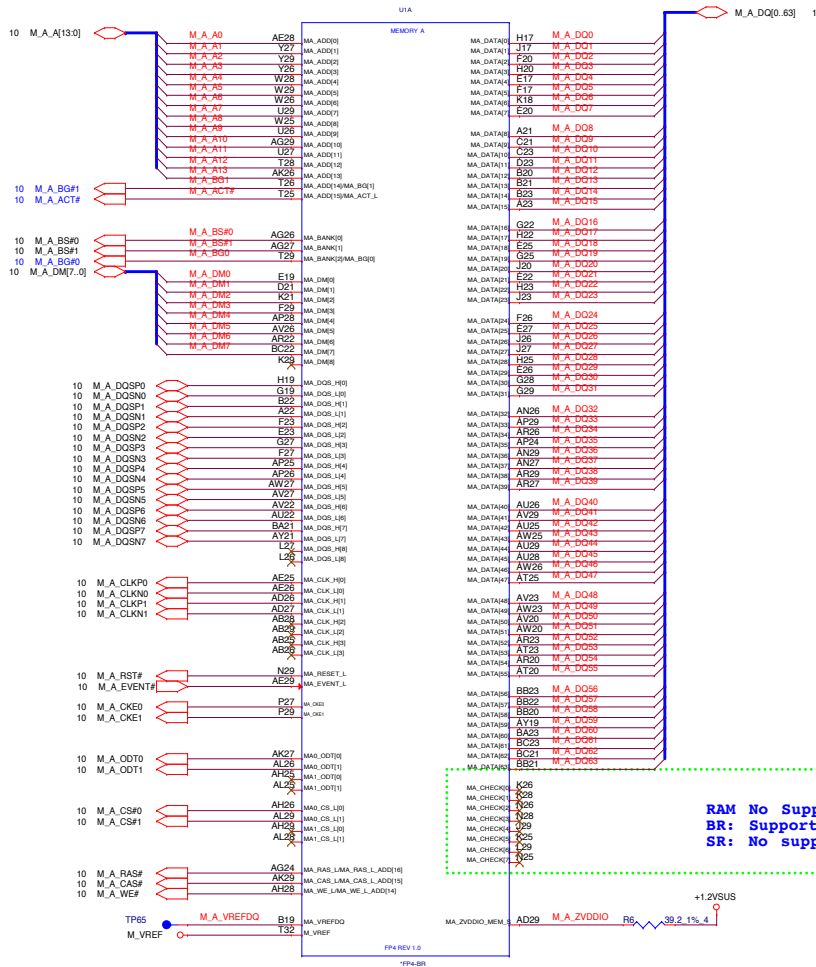
Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, January 16, 2017	Sheet	1 of 48



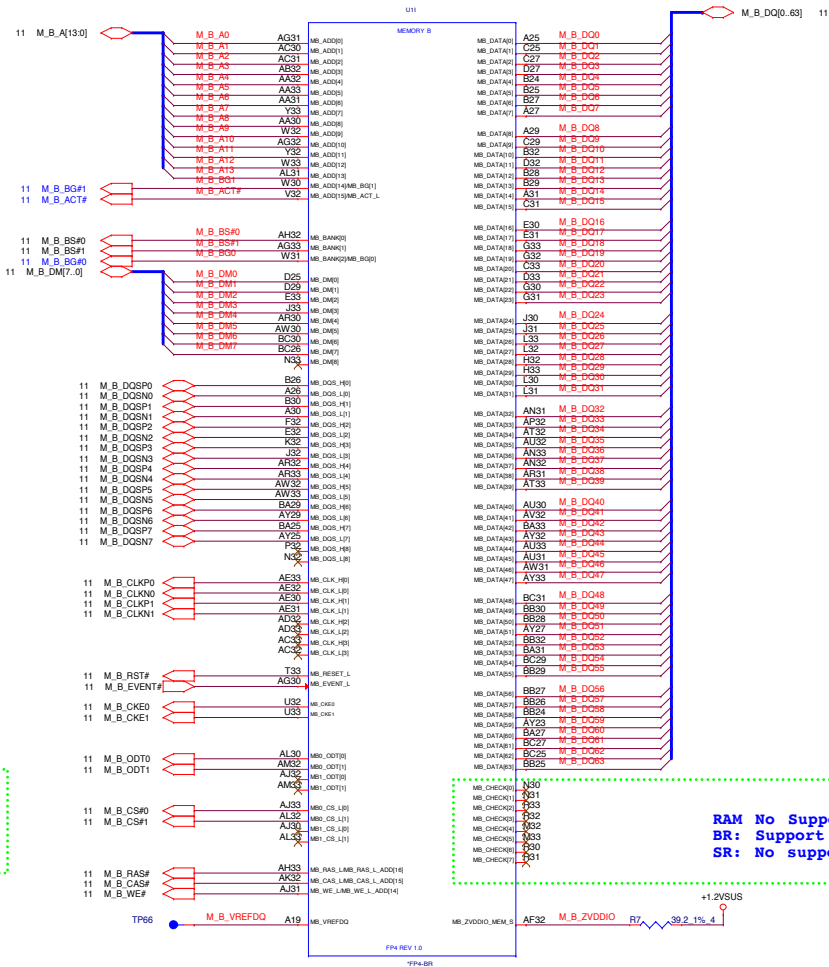
PROJECT:NFLP-G94A
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Size	Document Number	Rev
	BR & SR 1/7(PCIE)	1A
Date: Monday, January 16, 2017	Sheet 2 of 48	

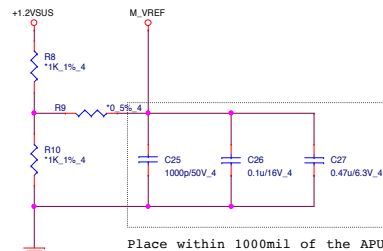
SB only channel B

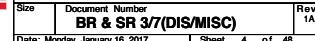


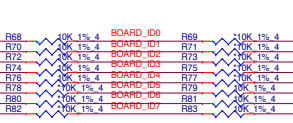
RAM No Support
BR: Support ECC
SR: No support ECC



RAM No Support
BR: Support ECC
SR: No support ECC







Board ID 0	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15.6" 15PD
10	17"
11	15.6" 25PD

Board ID [4:3]	Definition
00	PORT0 SATA only
01	PORT0 SATA PORT1 SSD
10	PORT0 SATA PORT1 ODD
11	PORT0 SATA PORT1 SSD USB3.0 to ODD

Board ID [5]	Definition
0/1	BR/SR

Board ID [6]	Definition
0/1	VRAM Size X8/ X4

Board ID [7]	GPU
0/1	M1-70/ M1-30

Board ID [9:8]	Definition
00	NFL-P
01	NFL-C
10	VINE-DF
11	Reserve

Board ID [10]	Definition
0/1	Reserve

Figure 10 shows the ACZ pin connections. The diagram includes the following components and connections:

- Pin 22 ACZ_SDOUT_AUDIO is connected to R119 (33 5% 4) and ACZ_SDOUT_R.
- Pin 22 ACZ_SYNC_AUDIO is connected to R120 (33 5% 4) and ACZ_SYNC_R.
- Pin 22 BIT_CLK_AUDIO is connected to R121 (33 5% 4) and ACZ_BCLK_R.
- Pin 22 ACZ_RST#_AUDIO is connected to EC1 (15050pV 4) and ACZ_RST#_R.
- Pin 22 ACZ_SIN0 is connected to R122 (33 5% 4) and ACZ_SIN0.

31,44,47 DGPU_PR_EN

R126 1k

C43 0.47uF 6.3V_4

Q5 MTRX213-G

DIS: Stuff
UMA: No Stuff

CLKREQ#

Node	Resistor Value	Resistor Tolerance	Resistor Count	Test
R113	2.2K	5%	4	APU_TEST0
R115	1K	1%	4	APU_TEST1
R117	2.2K	5%	4	APU_TEST2
R114	15K	1%	4	
R116	15K	1%	4	
R118	15K	1%	4	

TEST2	TEST1	TEST0	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted. FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

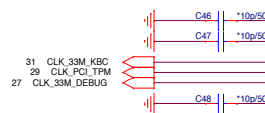
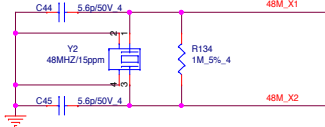
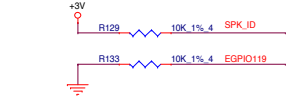
5,7,25,27,30,31,34,35,37,42,43,44,47
7,26,42
4,5,7,10,11,20,21,22,24,26,27,28,29,30,31,38,40,43
7,31,43

+3VSS
+0.95VSS
+3V
+1.8V_ROM



Follow Checklist

OPTION: ODD or SSD(M.2)

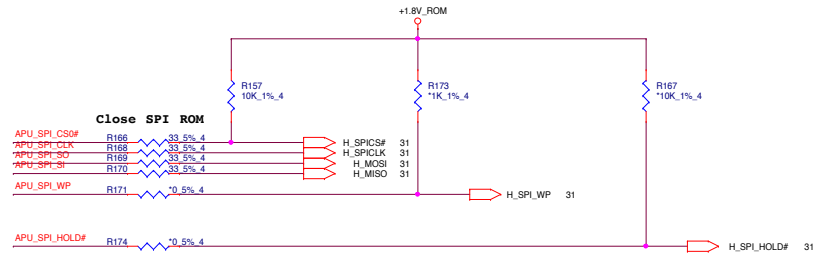


For EMI



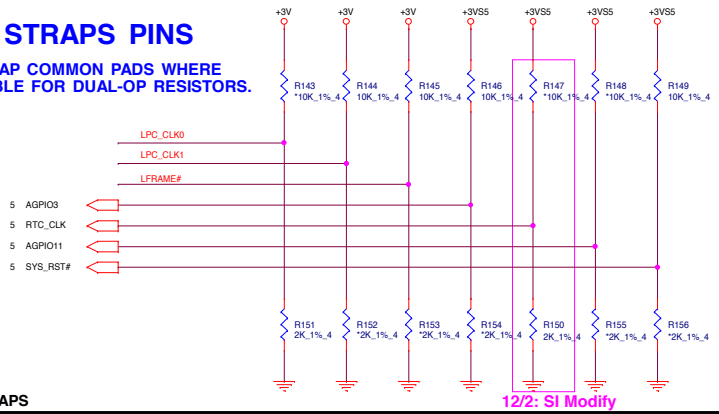
APU SPI ROM

Vender	Size	P/N (1.8V)
WND	8M	AKE5EZNO00
EON	8M	AKE5EFNO000
	8M	
Socket	DFHS08FS023	



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 Int Pull-Up	RTC_CLK Int Pull-Up	AGPIO11=BLINK Int Pull-Up	SYS_RST# Int Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM Enhanced reset logic (for quicker SS resume) DEFAULT	Coin battery is on board. DEFAULT	LDT_RST#/LDT_PWRGD output to APU DEFAULT	normal reset mode DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100Mhz PCIE clock as reference clock and generate internal clocks only DEFAULT	LPC ROM DEFAULT	3.3V SPI ROM Default to traditional reset logic DEFAULT	Coin battery is not on board. DEFAULT	LDT_RST#/LDT_PWRGD output to Pads DEFAULT	short reset mode DEFAULT

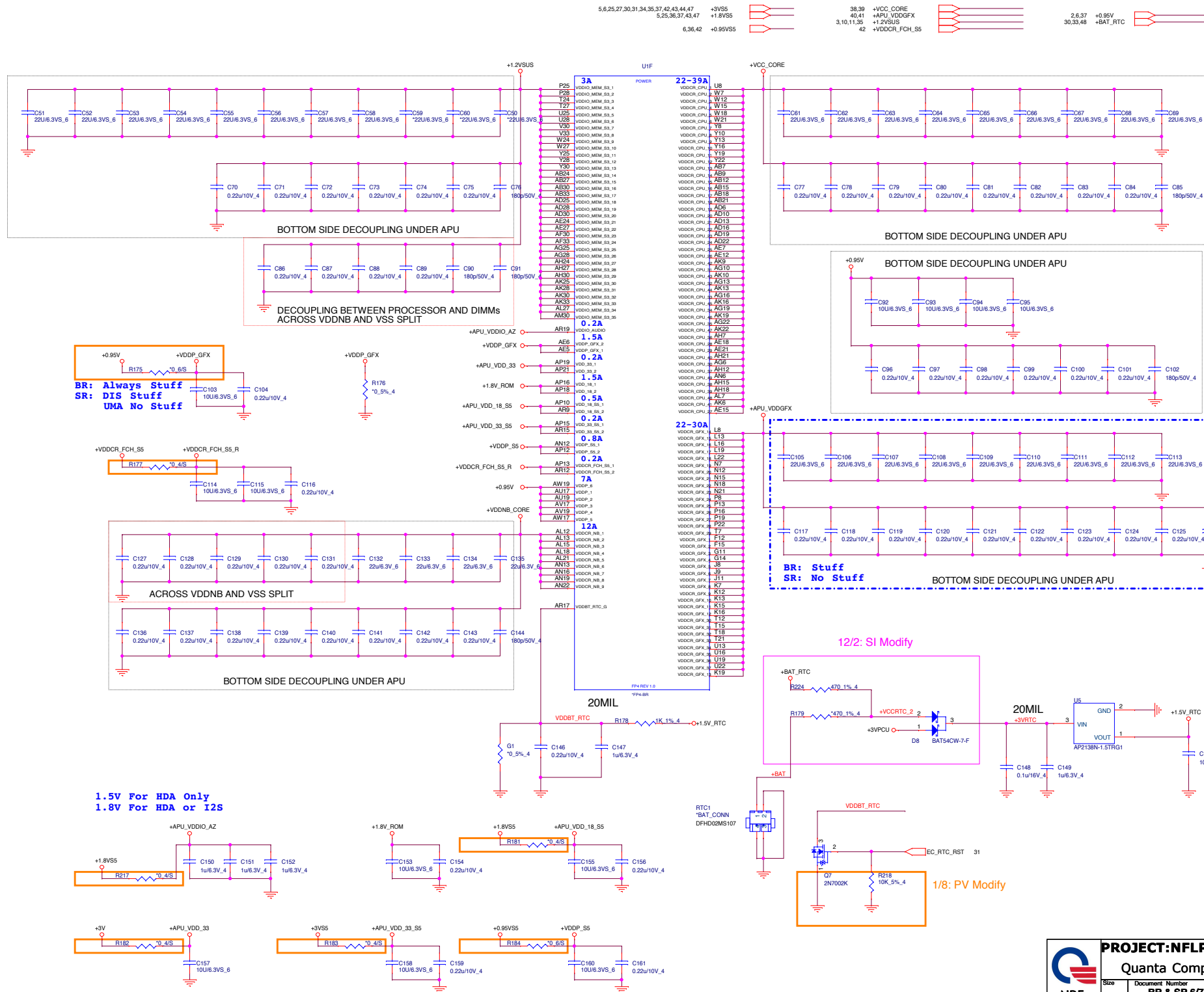


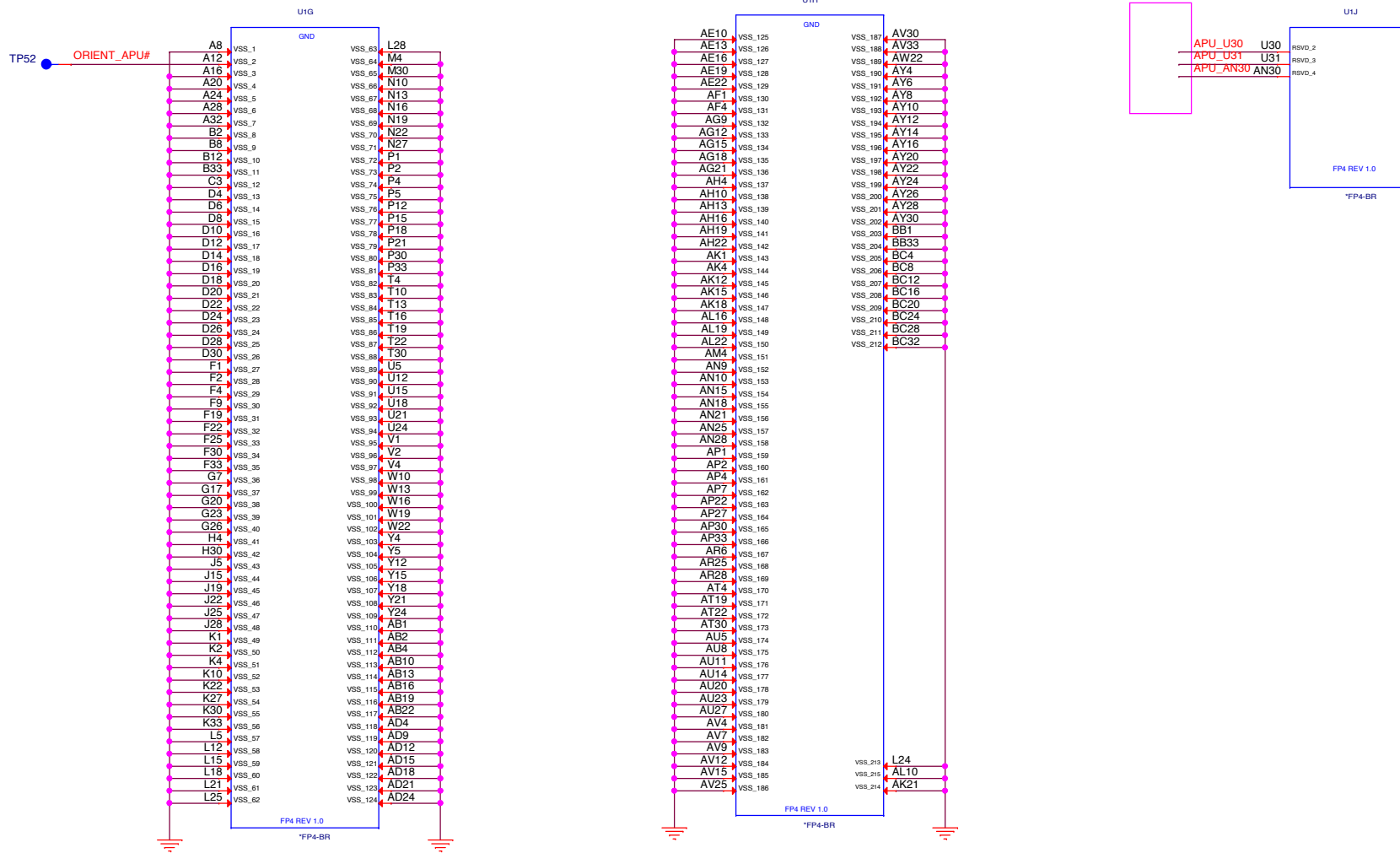
PROJECT:NFLP-G94A

Quanta Computer Inc.

Size	Document Number	Rev
6	BR & SR 5/7(SATA/USB/SPI)	1A

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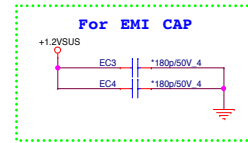
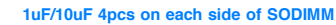


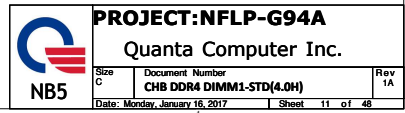
**PROJECT:NFLP-G94A**

Quanta Computer Inc.

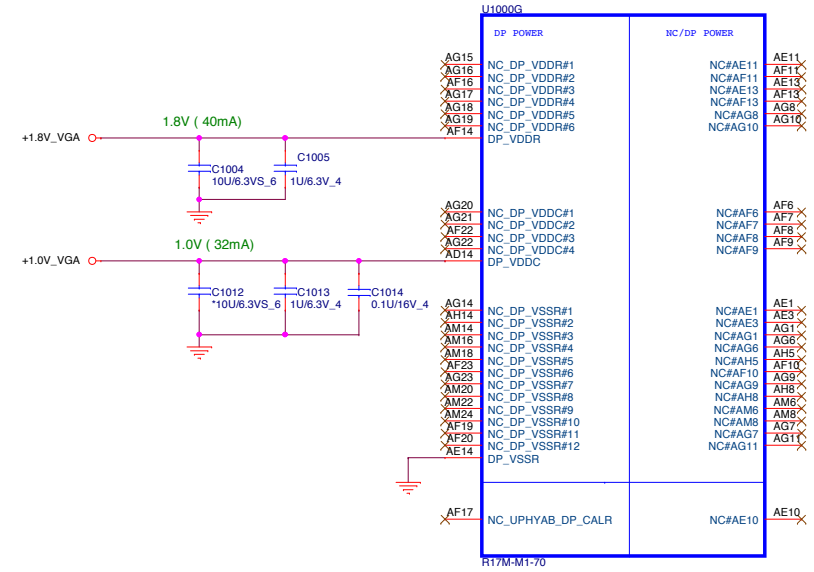
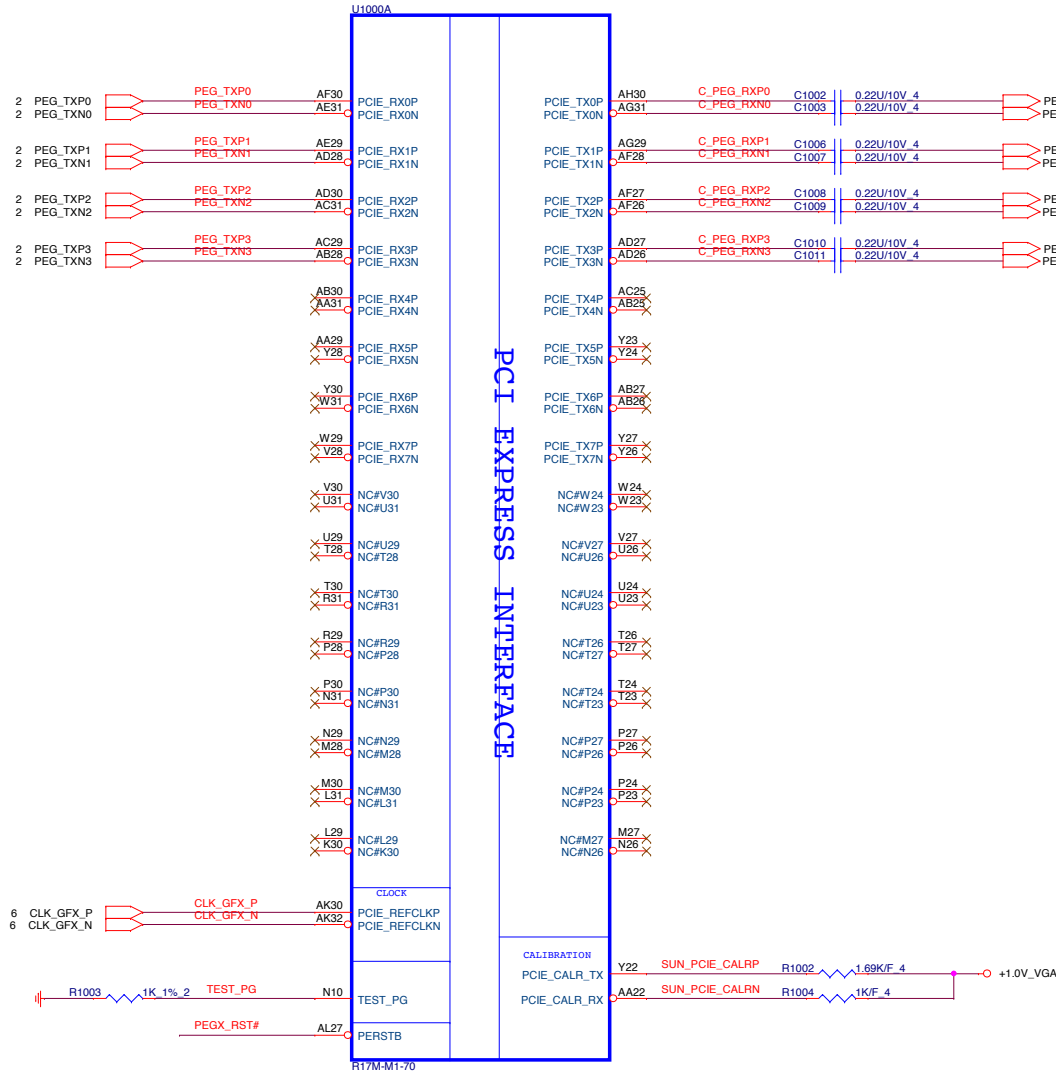
Size	Document Number	Rev
	BR & SR 7/7 (GND)	1A
Date: Monday, January 16, 2017	Sheet 8 of 48	

<Reserved>

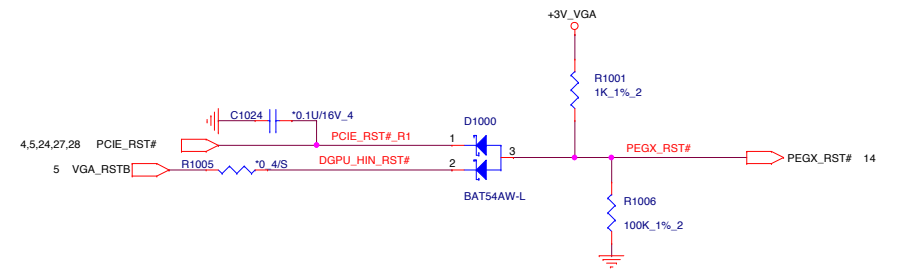




14,16,43,44,47 +3V_VGA
14,16,43,44,47 +1.8V_VGA
16,43,47 +1.0V_VGA



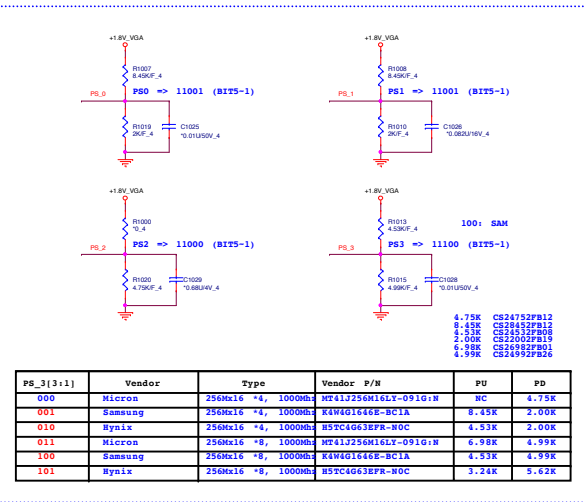
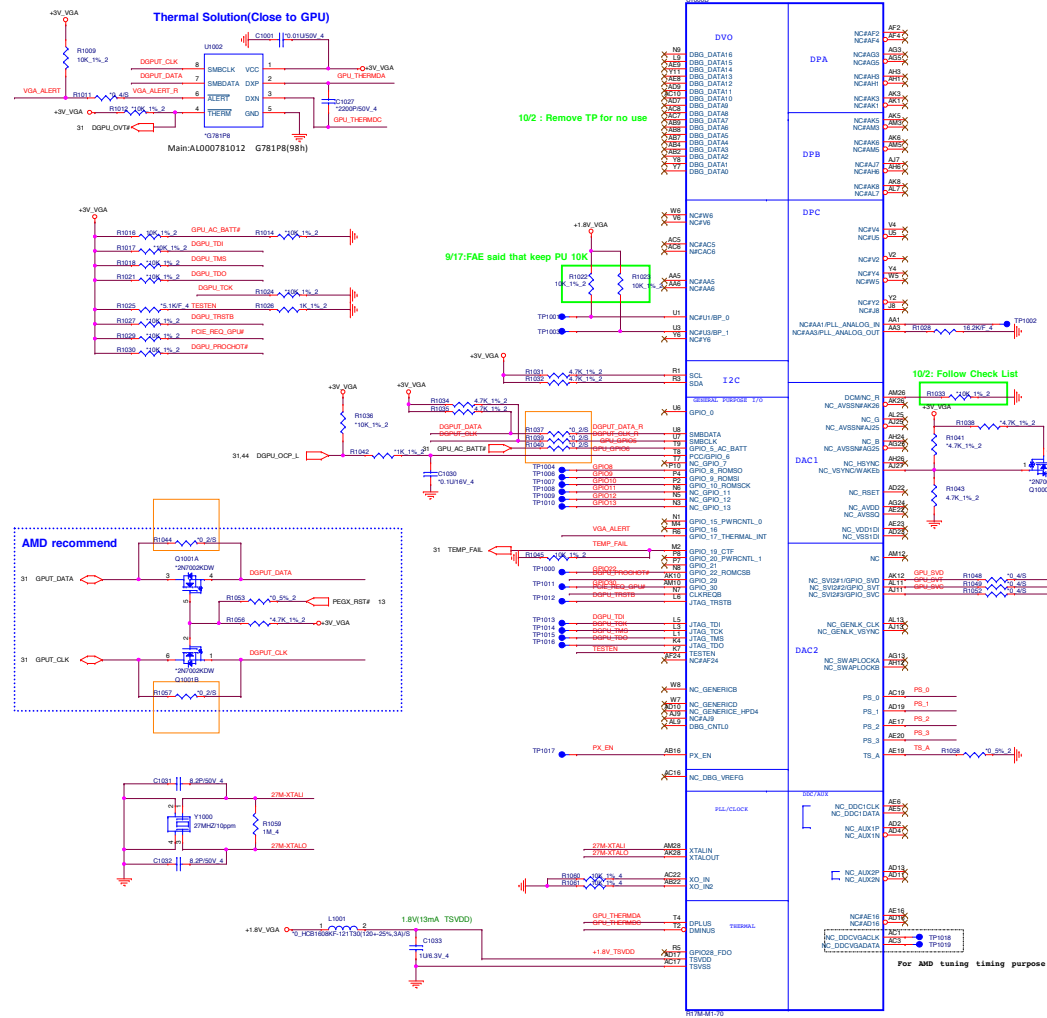
GPU Reset Signal



PROJECT:NFLP-G94A

Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_PCIE/DP POWER	1A
Date: Monday, January 16, 2017	Sheet	13 of 48



- **MIPS Implementation**
 - Connect GPIO_28 to 10K pulldown to enable MIPS
 - If any of PS_0/1/2/3 is not used, leave "no connect"
 - R_{pu}, R_{pd} and C_u must be properly populated per tables below
 - Place MIPS circuit components as close to the ASIC as possible
 - Total DC resistance of trace between PS pin and C should be less than 100Ω
 - Total DC resistance of trace between C and ground should be less than 100Ω
 - Trace capacitance should be less than 100pF. Resistors should be tolerance

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

R _{pu} (Ωm)	R _{pd} (Ωm)
NC	4750
8450	2000
4530	2000
6980	4990
4530	4990
3240	5620
3400	10000
4750	NC

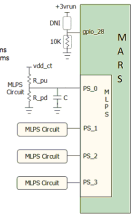
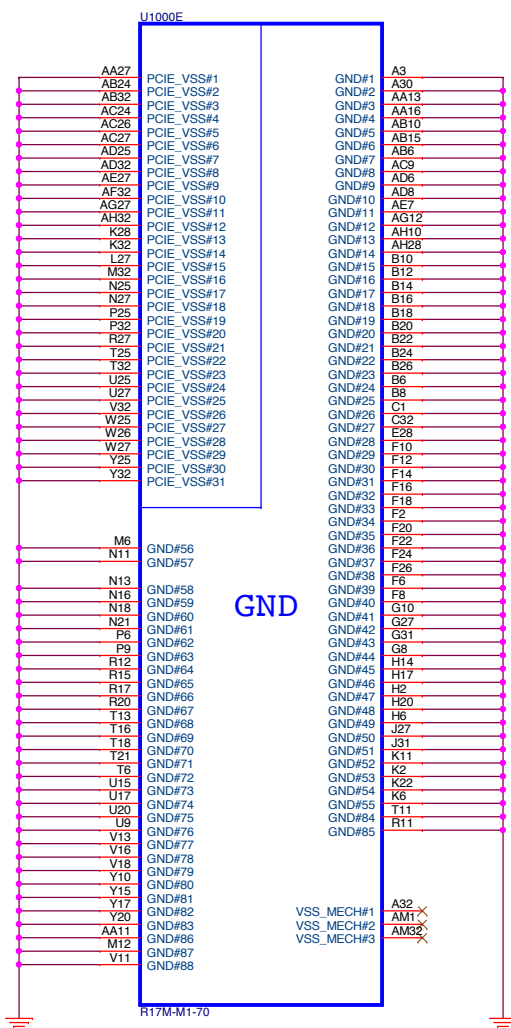


Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLPS bit	String Name	Description	Recommended Settings
PS_001	ROM_CFGF0H	If STRAP_BIOS_ROM_EN = 1, ROM_CFGF0H defines the ROM type.	Design dependent, see the description.
PS_002	ROM_CFGF1H	1 = PC16 GEN3 is supported. 0 = PC16 GEN3 is not supported.	
PS_003	ROM_CFGF2H	Determines whether or not the PC16 reference clock power management capability is reported (otherwise known as CLKREQ#).	
PS_004	N/A	Reserved for internal use only. Must be 0 at reset.	1
PS_005	N/A	Reserved.	1
PS_101	STRAP_BIF_GEN3_EN_A	PC16 GEN3 capability. 1 = PC16 GEN3 is supported. 0 = PC16 GEN3 is not supported.	Design dependent, see the description.
PS_102	STRAP_BIF_CLK_PEN_EN	The CLKREQ# power management capability is disabled. 1 = The CLKREQ# power management capability is enabled.	0
PS_103	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_104	STRAP_TX_CFG_DP_FULL_SWING	Control the transmitter full-swing mode. 0 = The transmitter half swing is enabled. 1 = The transmitter full swing is enabled.	1
PS_105	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter de-emphasis enable. 0 = Tx de-emphasis disabled. 1 = Tx de-emphasis enabled.	Design dependent, see the description.
PS_201	N/A	Reserved.	0
PS_202	N/A	Reserved.	0
PS_203	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_204	N/A	Reserved.	1
PS_205	N/A	Reserved.	1
PS_301	BOARD_CFGF0G0	Board configuration related strapings, such as for memory ID.	Design dependent, see the description.
PS_302	BOARD_CFGF1G0		
PS_303	BOARD_CFGF2G0		
PS_304	N/A	Reserved.	1
PS_305	N/A	Reserved.	1



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

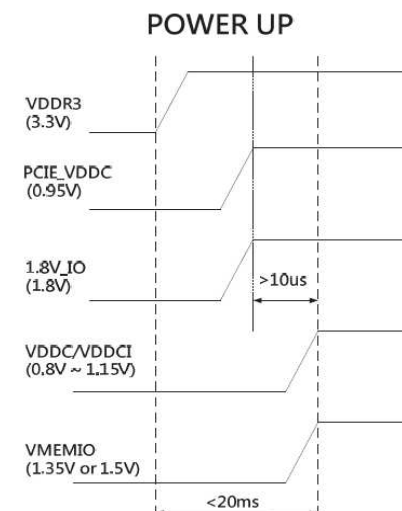
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

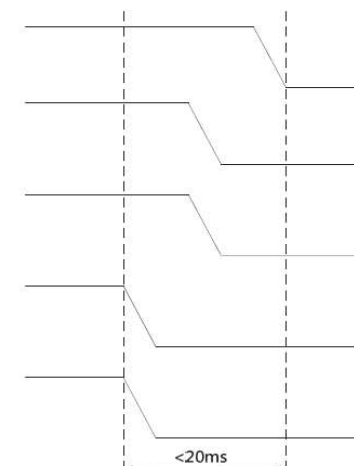
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE



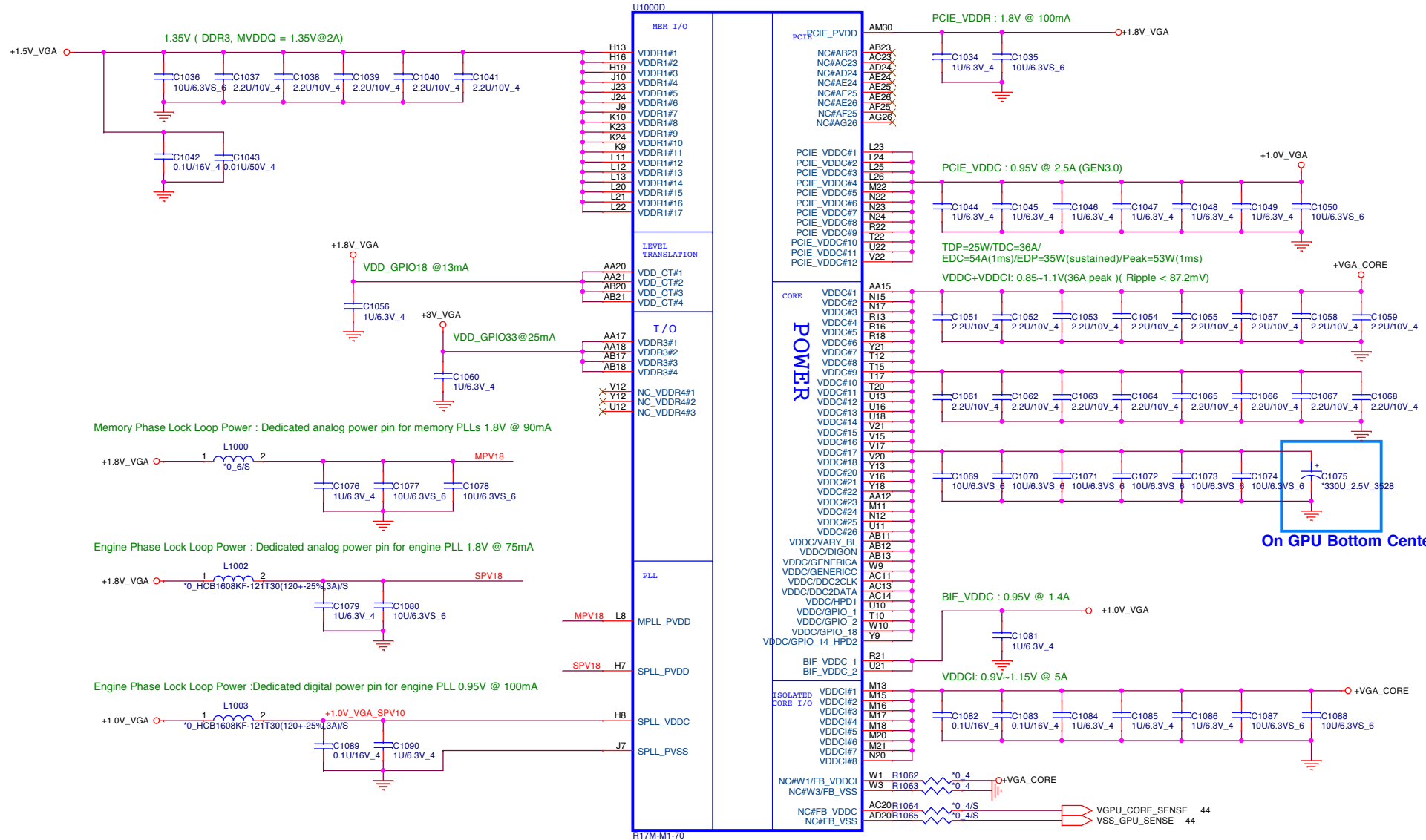
POWER DOWN

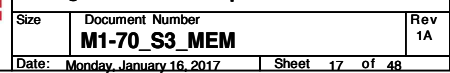


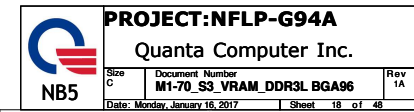
PROJECT:NFLP-G94A

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Size	Document	Number	Rev
	M1-70_S3_GND/LVDS/Strap		1A
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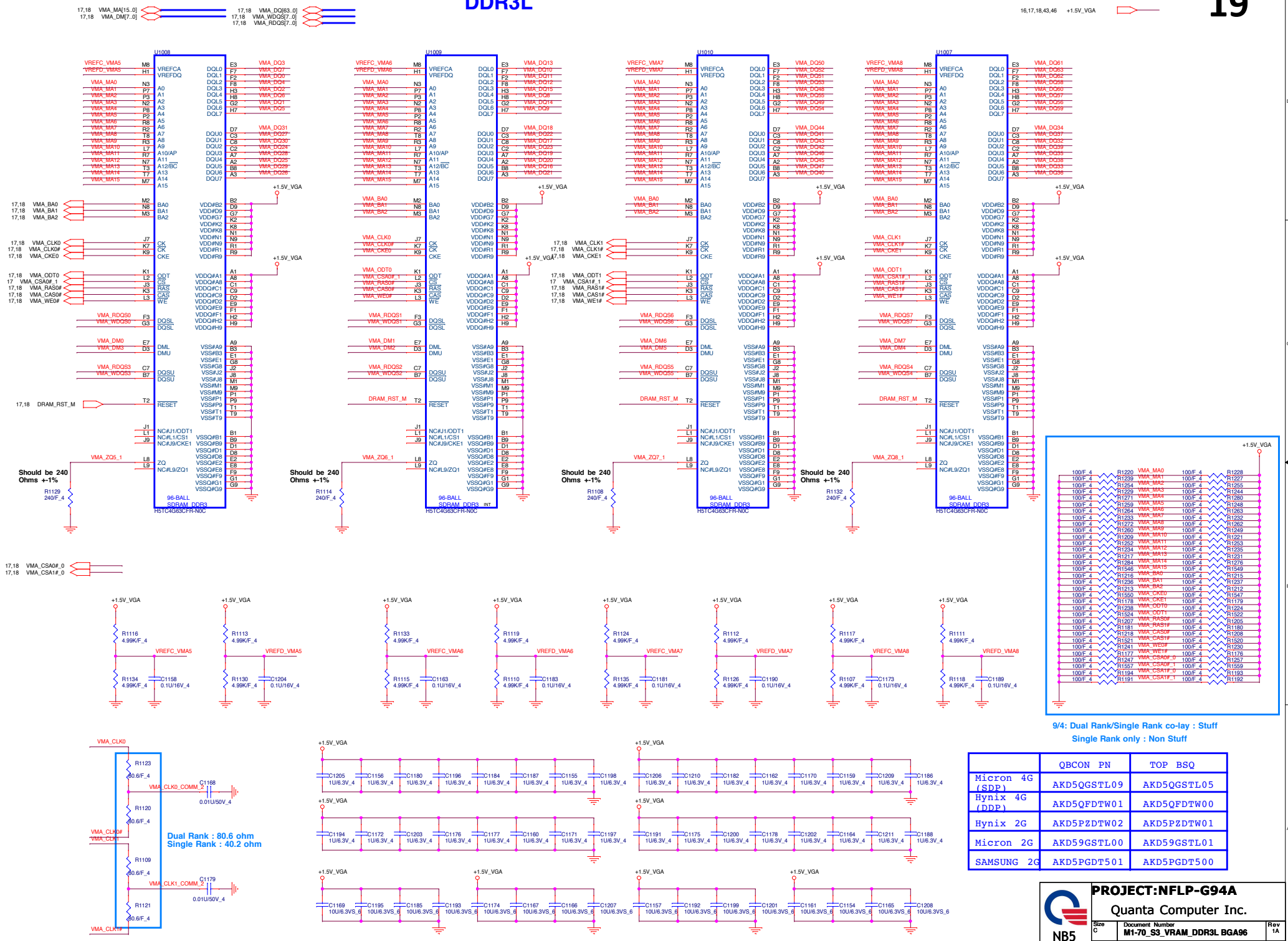






DDR3L

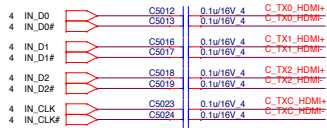
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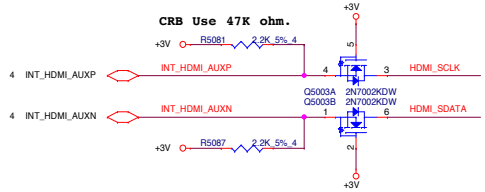
9/4: Dual Rank/Single Rank co-lay : Stuff
Single Rank only : Non Stuff

	QBICON PN	TOP BSQ
Micron 4G (SDP)	AKD5QGSTL09	AKD5QGSTL05
Hynix 4G (DDP)	AKD5QFDTW01	AKD5QFDTW00
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

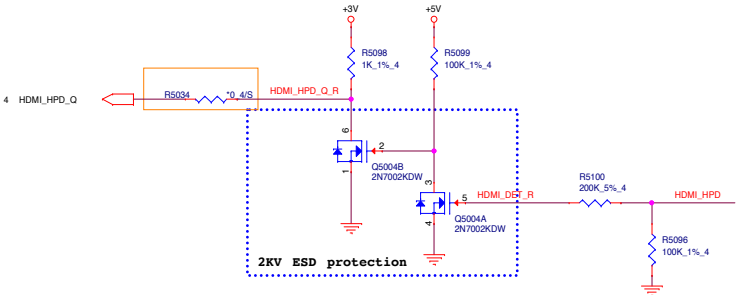
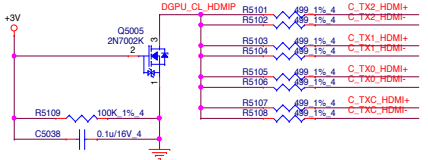
HDMI CONN



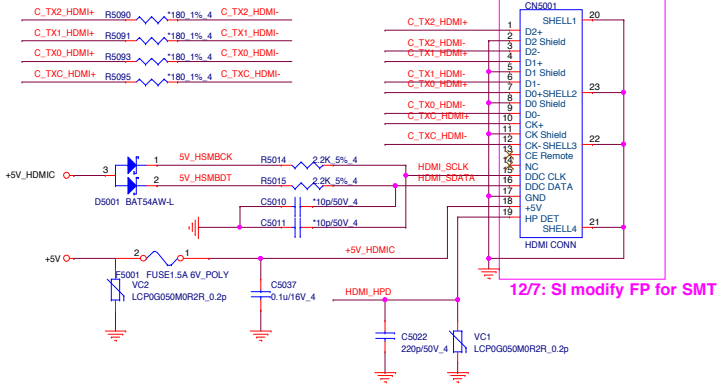
HDMI SMBus isolation



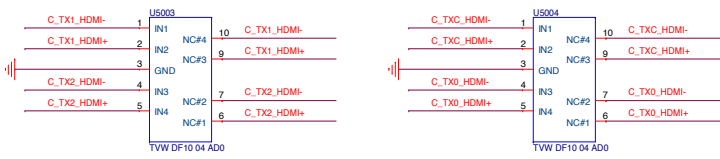
Close to HDMI connector



For EMI Solution



For ESD Solution

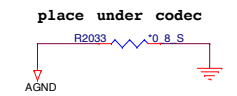
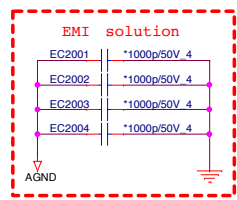
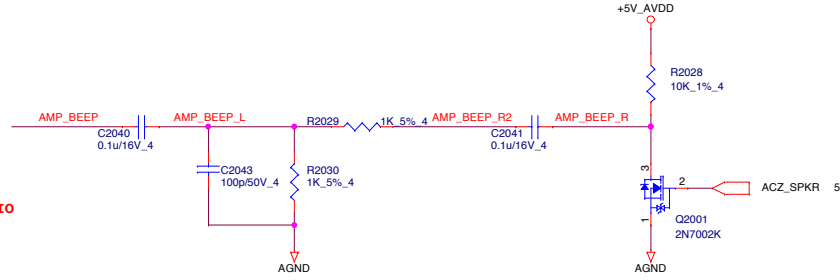
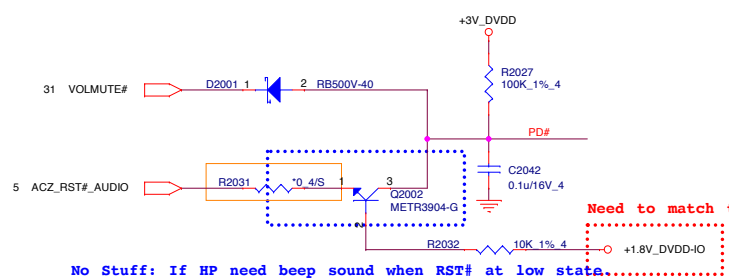
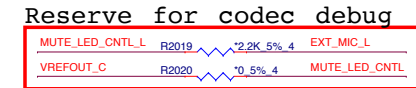
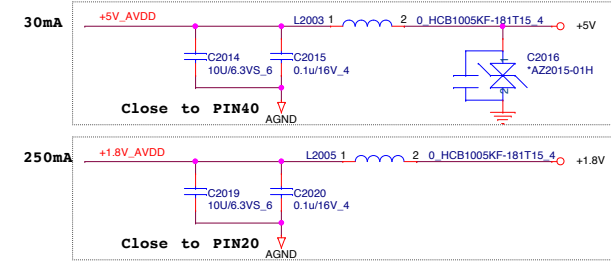
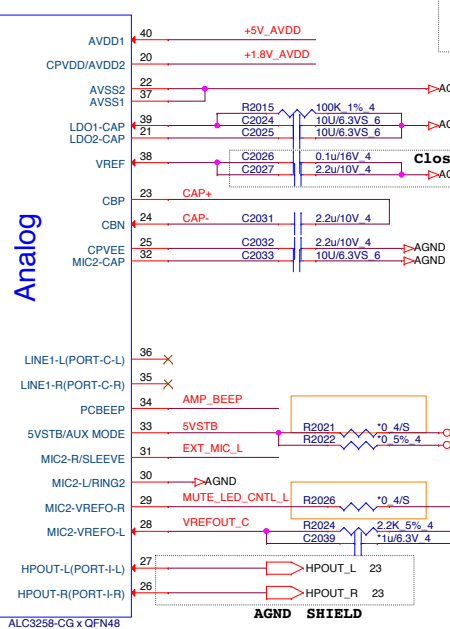
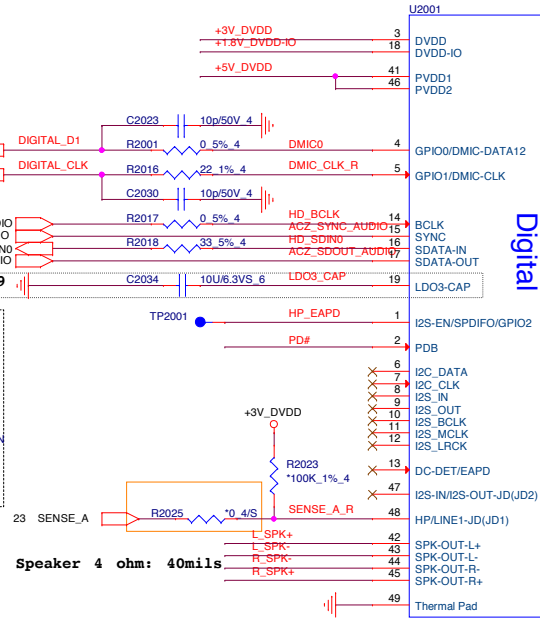
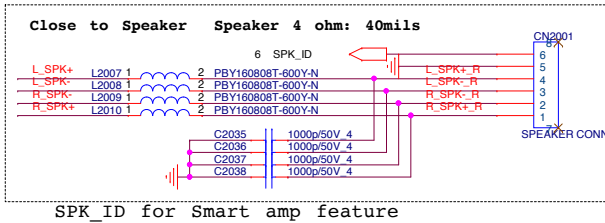
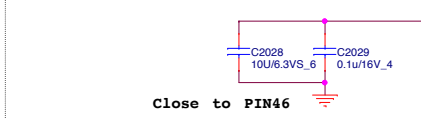
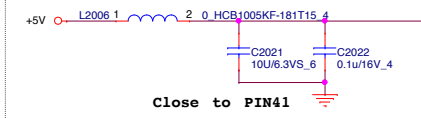
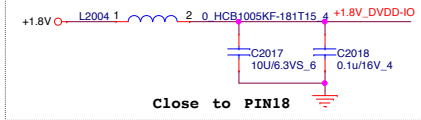
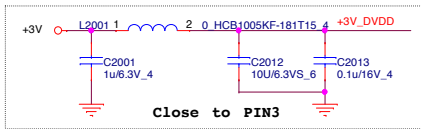


Audio ALC3258-CG

20,21,26,30,43 +5V
4,5,6,7,10,11,20,21,24,26,27,28,29,30,31,38,40,43 +3V
4,5,25,26,38,40,43 +1.8V



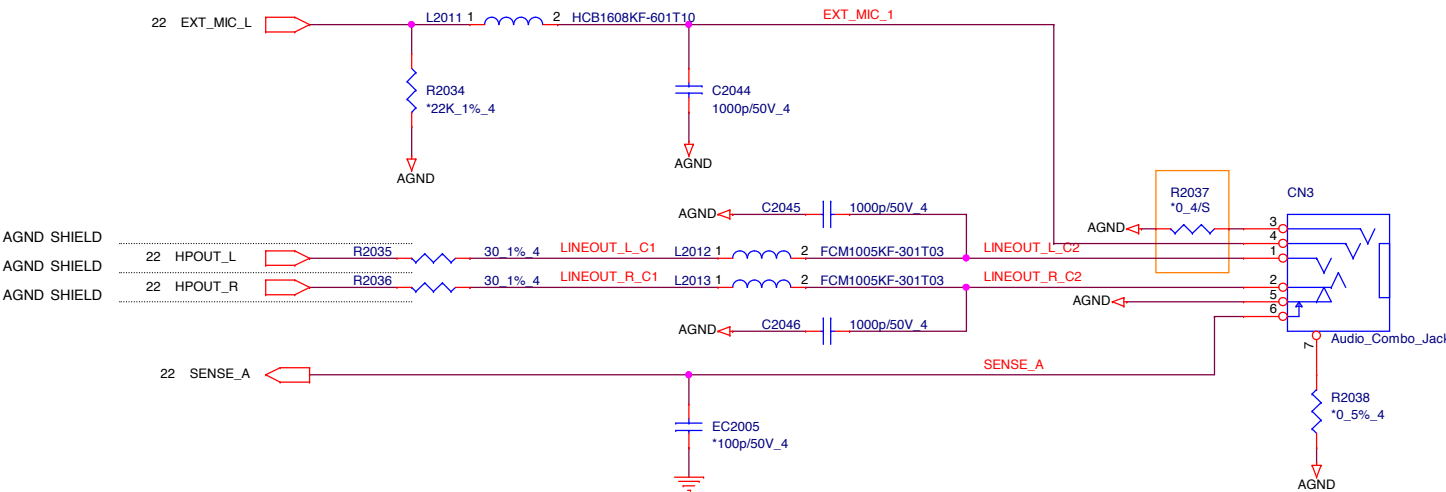
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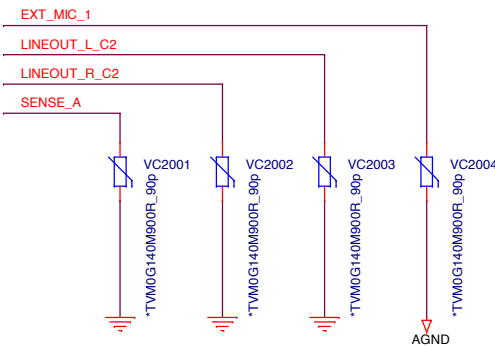
PROJECT:NFLP-G94A

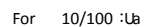
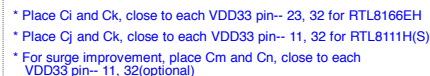
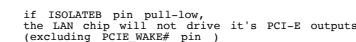
Quanta Computer Inc.

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Audio ALC3258-CG		
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Audio JACK ESD





```
1st source :NS681684 DBOLE6LAN20
2nd source :NS0013B LF DBOLE6LAN0
```

For Giga :Ub

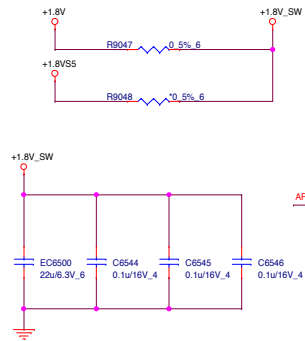
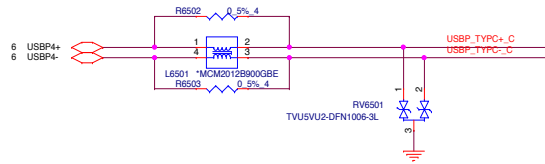
For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 .DB0LL1LAN00



PN change, FP the same

USB3 SW - PI2EQX632 + USB TYPE-C - TPS25810

USB2.0



SEL = High, Channel 1 active

SEL = NC, Both Channels are Power-down

SEL = Low, Channel 2 active

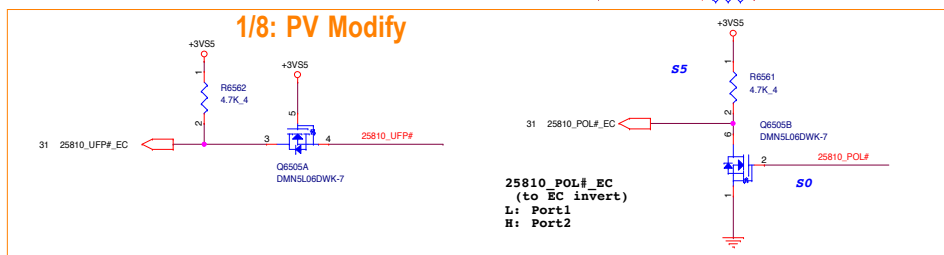
1/12: Add Net name

11/27: SI change Pin define & Symbol error

USB3.0 SW

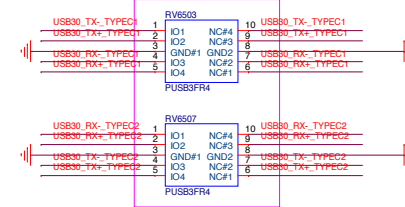
12/6: SI change U6501 FP for SMT

1/8: PV Modify



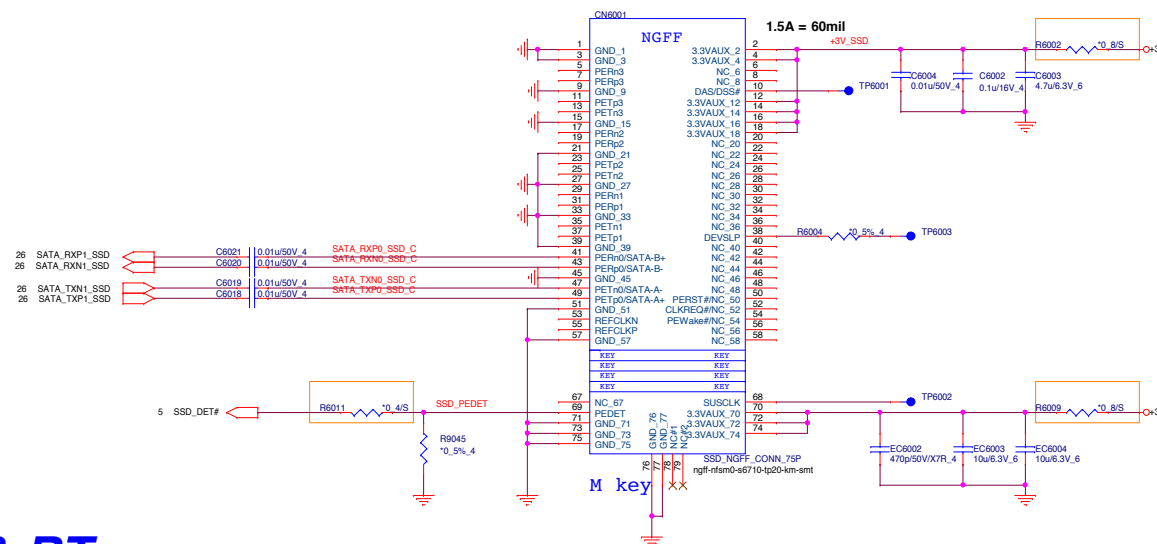
TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

TYPE C USB3.0 ESD

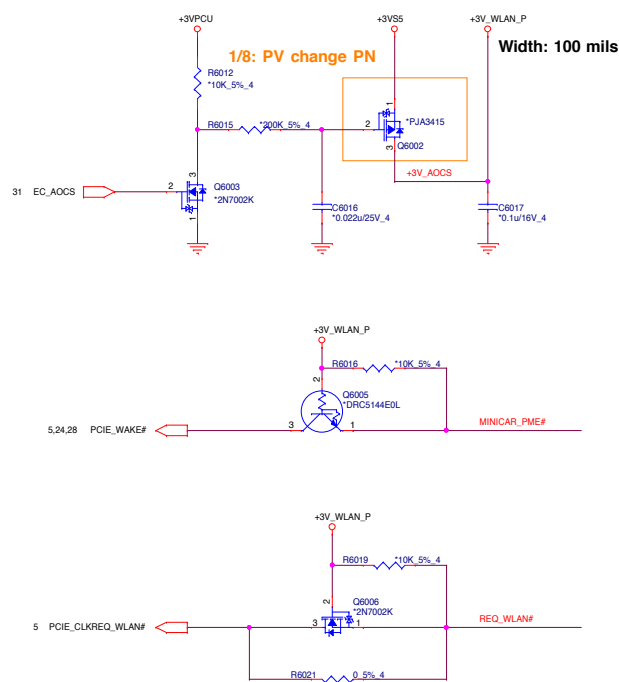


12/6: SI Modify FP/PN

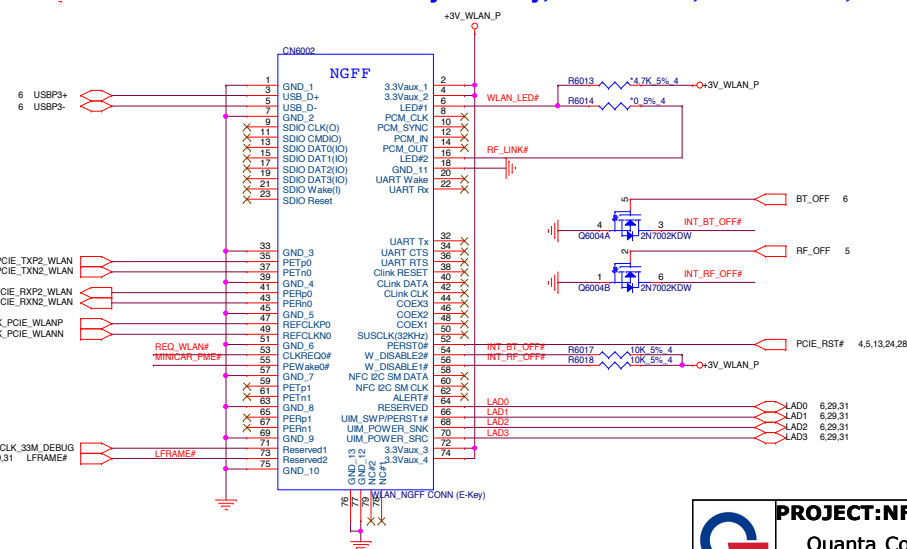
Conn PN FP OK! Libray modify, add Pin78,79



WLAN & BT

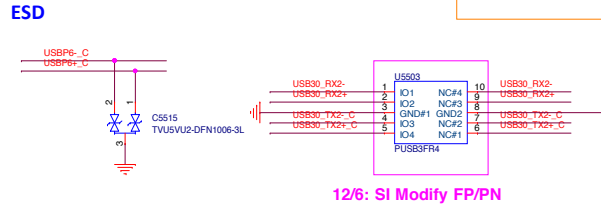
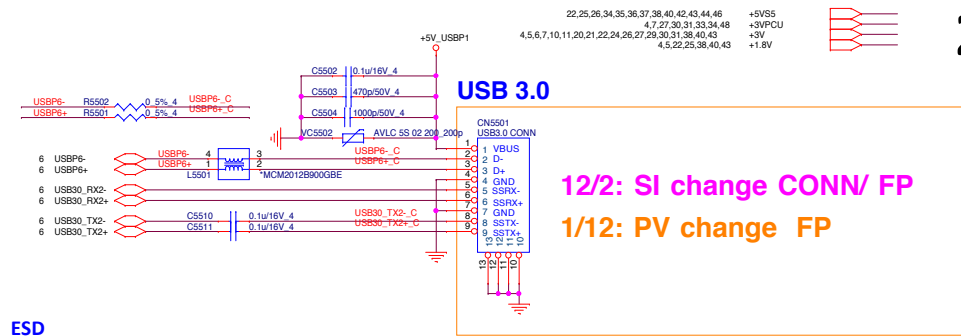
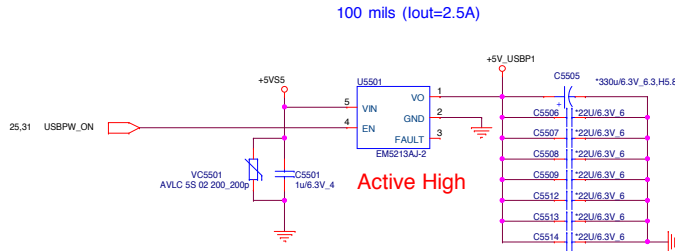


Conn PN FP OK! Library modify, Del 24~31, add Pin78,79



For 15.6" / 17.3" 2SPD

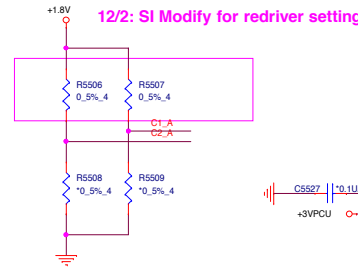
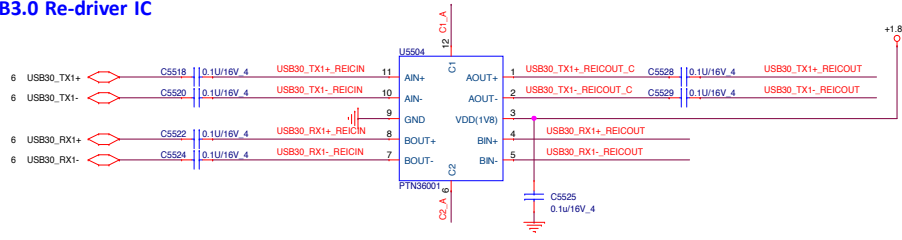
28



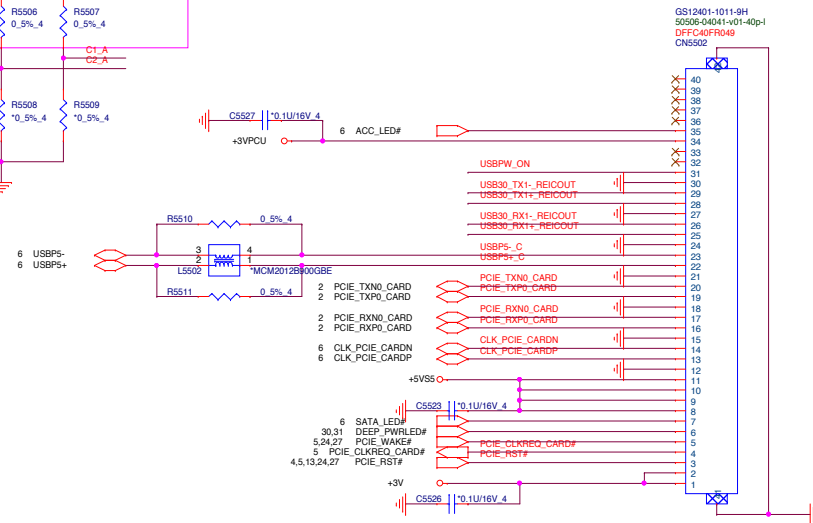
USB3.0

USB3.0 Re-driver IC

USB3.0 re-driver IC

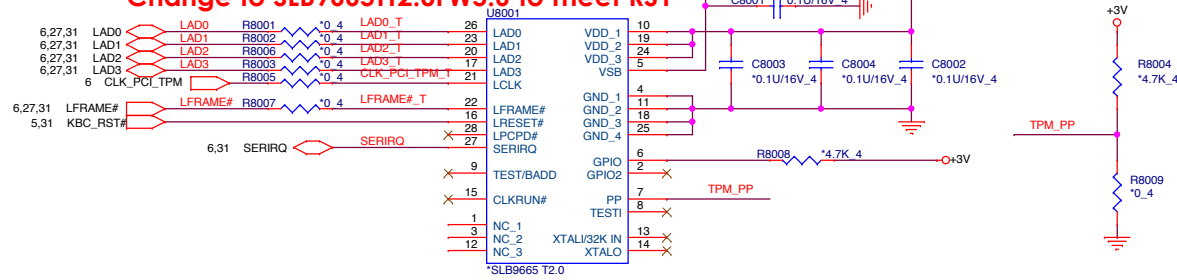


Confirm Library!



TPM (2.0)

Change to SLB9665T2.0FW5.6 to meet RS1



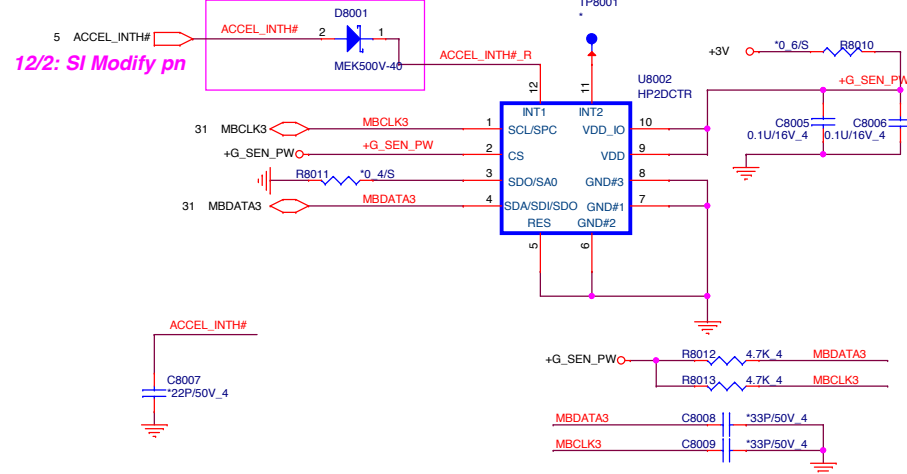
4,5,6,7,10,11,20,21,22,24,26,27,28,30,31,38,40,43

+3V_WLAN_P
+3V



29

Accelerometer Sensor

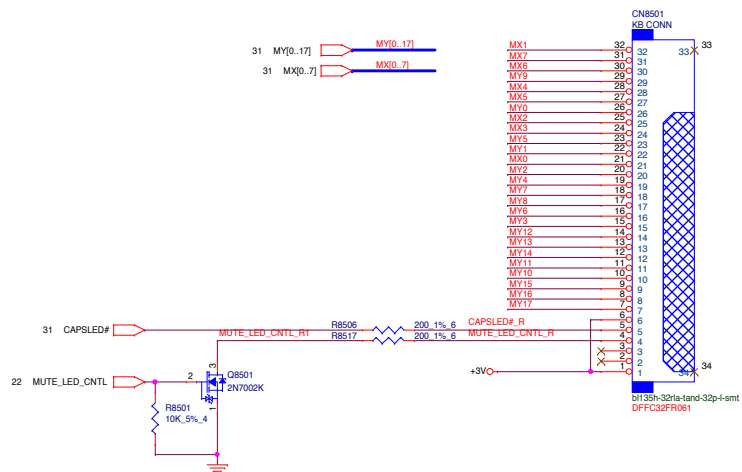


IR CAM on Page20

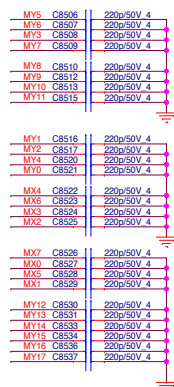
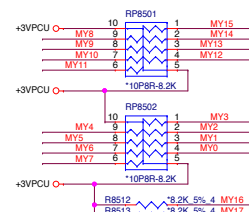
KEYBOARD CONN

Conn Wait confirm FP!!

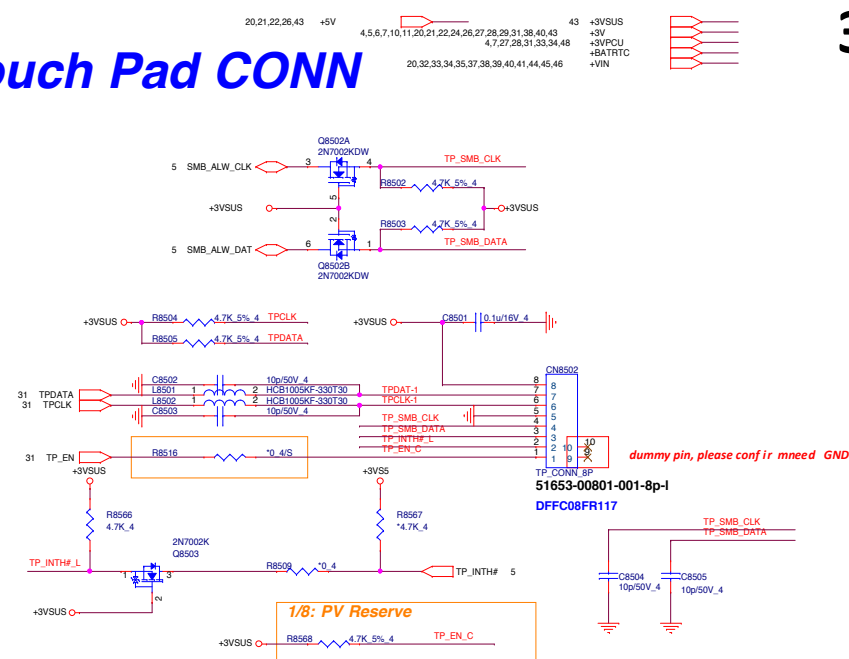
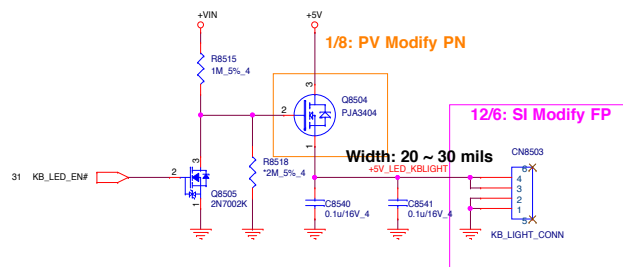
Touch Pad CONN



KEYBOARD PULL-UP

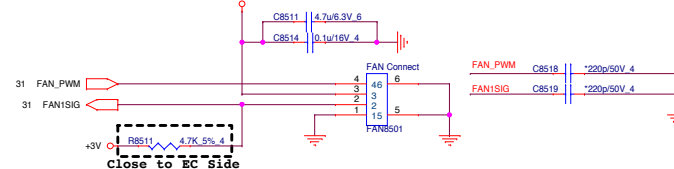


KB LIGHT CONN



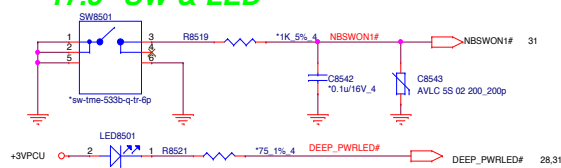
FAN CONN

confirm Library

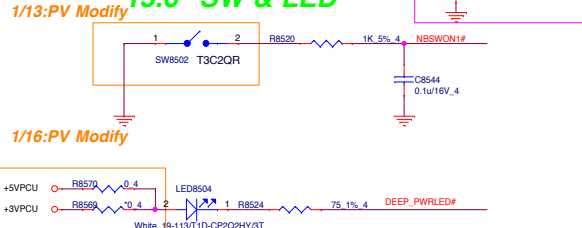


PWR Button & LED & HALL IC

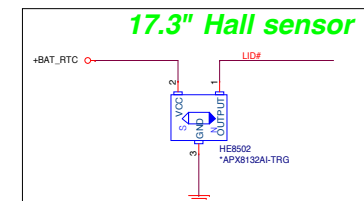
17.3" SW & LED



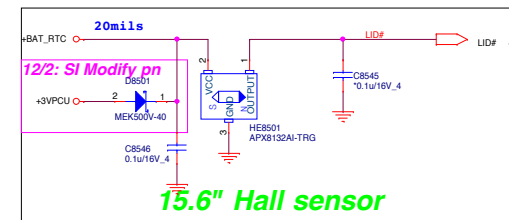
15.6" SW & LED

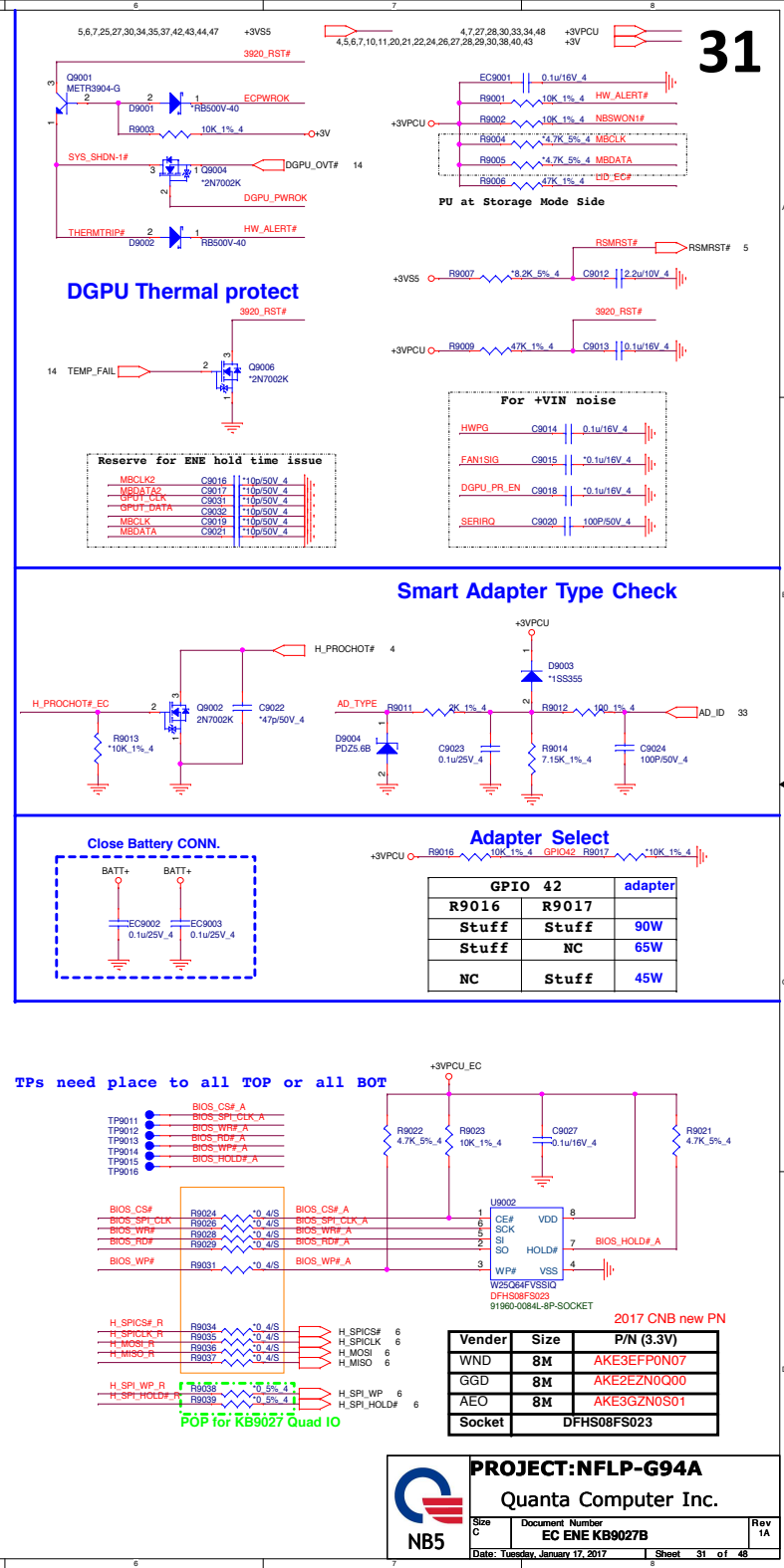
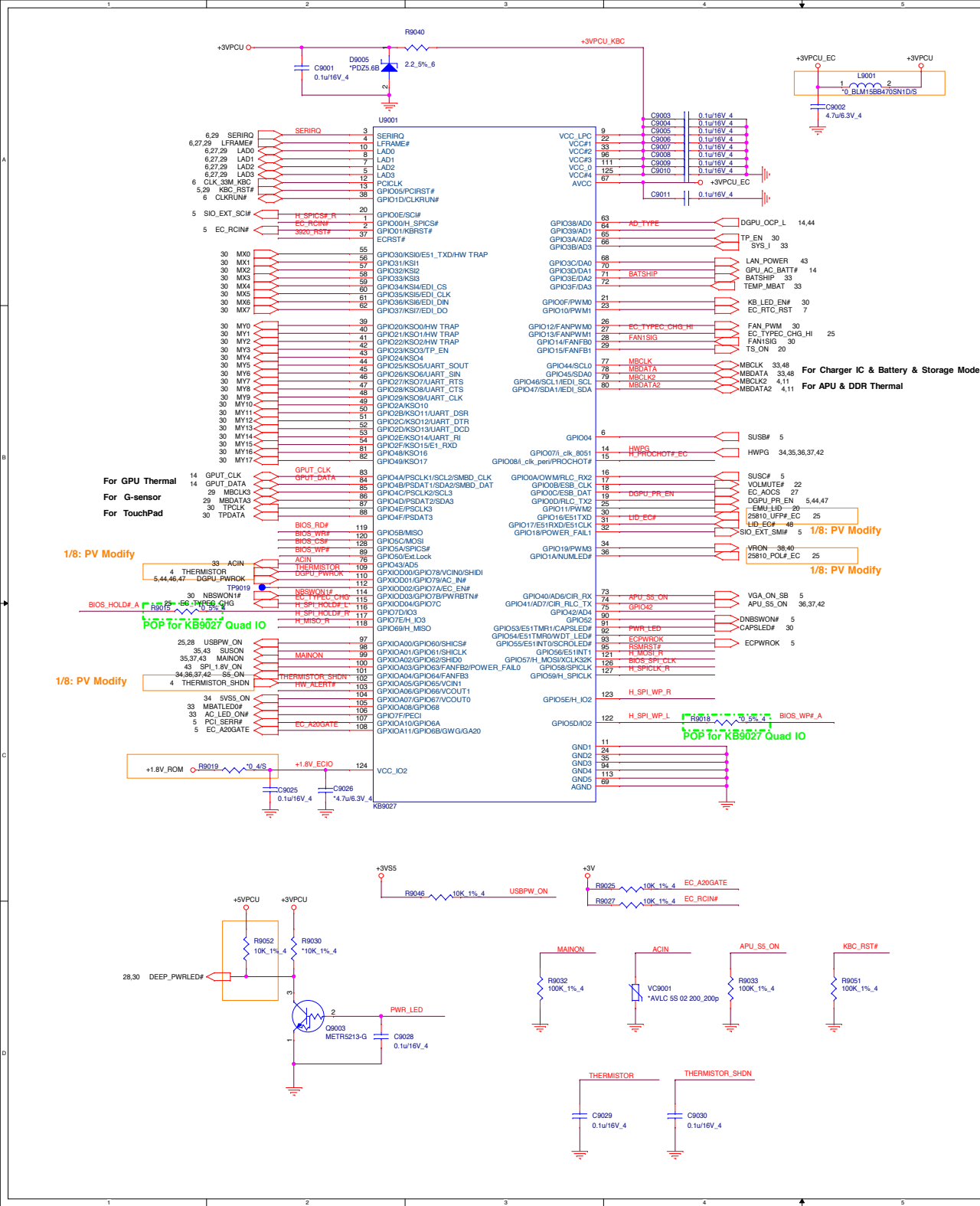


17.3" Hall sensor



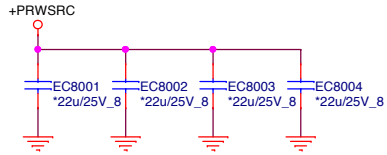
 15.6" Hall sensor



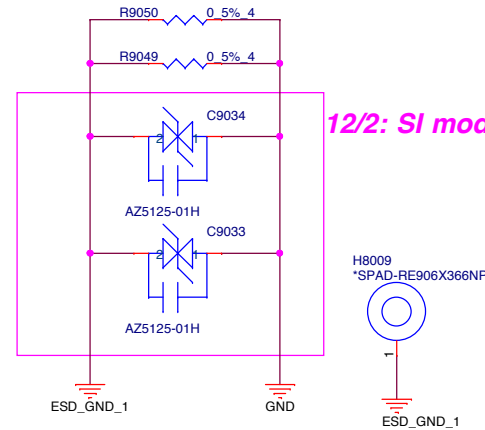
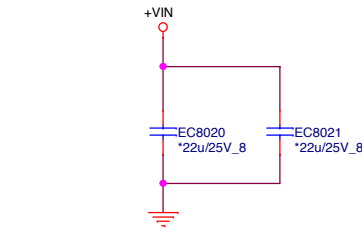
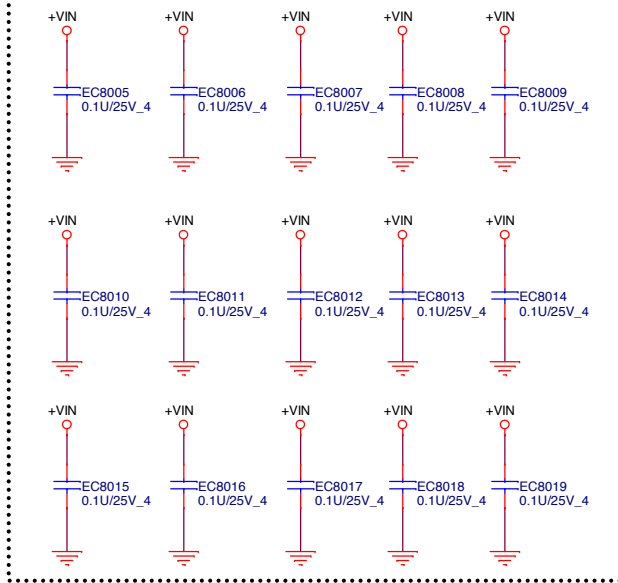


EMI CAPs

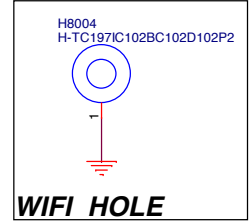
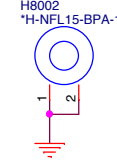
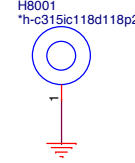
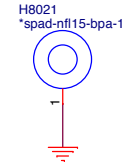
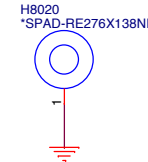
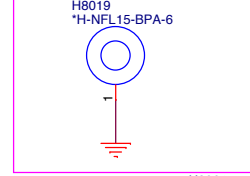
For ISN



Place on +VIN Path

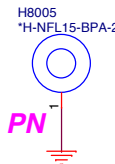
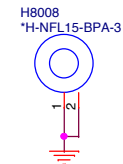
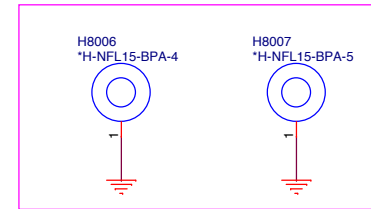


12/6: SI modify PN

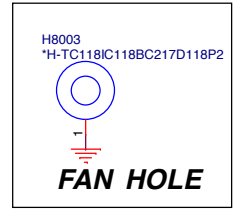
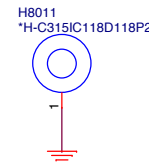
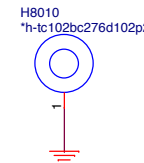
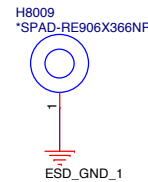


WIFI HOLE

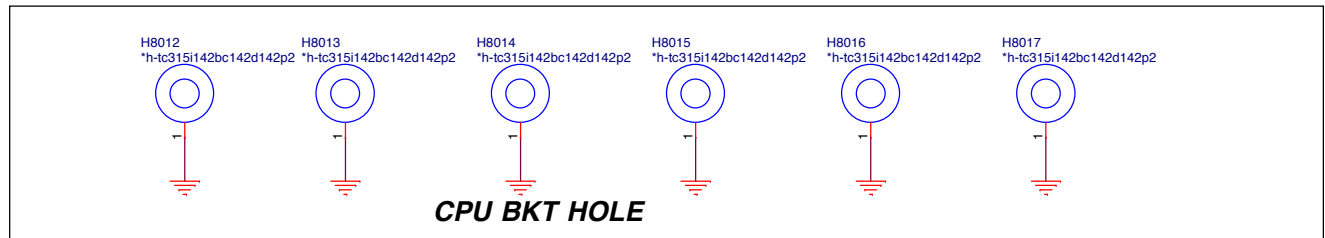
12/6: SI modify PN



12/2: SI modify PN



FAN HOLE



CPU BKT HOLE



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Quanta Computer Inc.

Size B	Document Number	Rev
	EMI CAP/HOLES	1A
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Do Not add test pad on BQBATDRV/BATDIS_ID_DOD signal

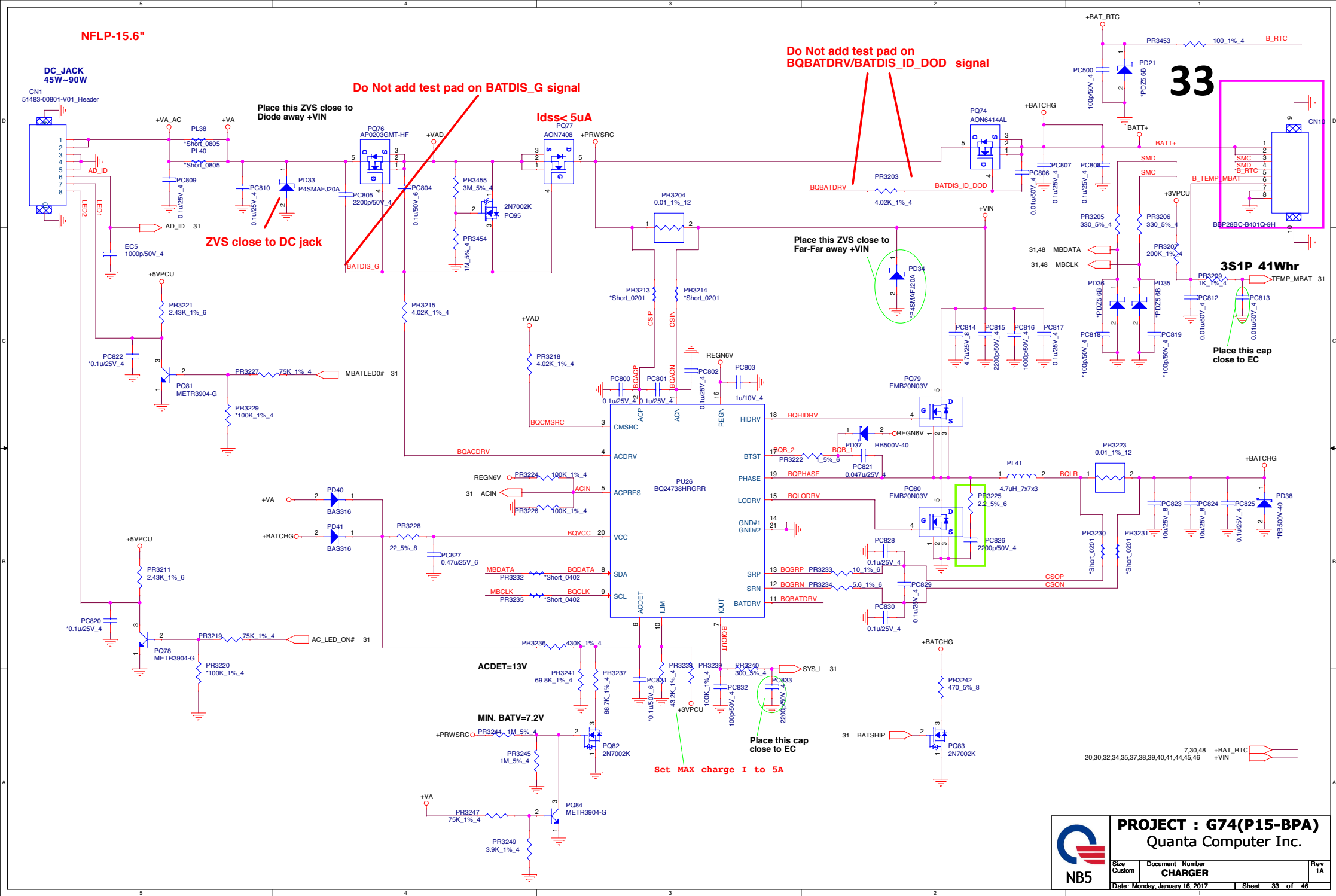
Place this ZVS close to
Far-Far away +VIN

33

3S1P 41W hr

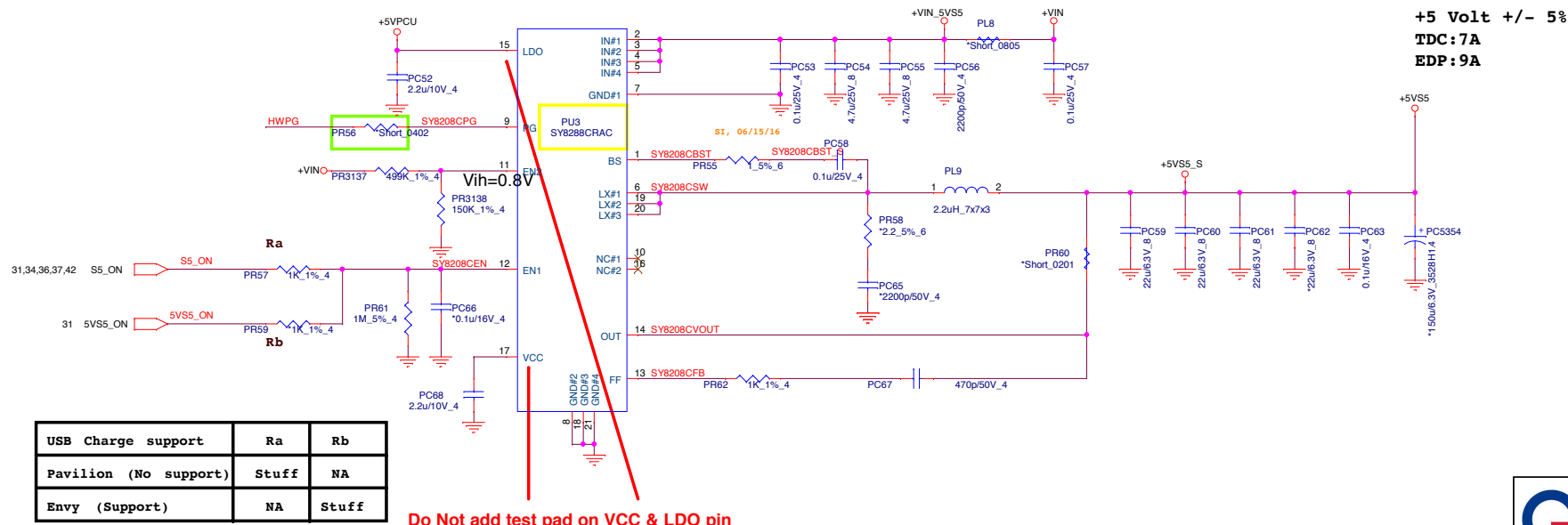
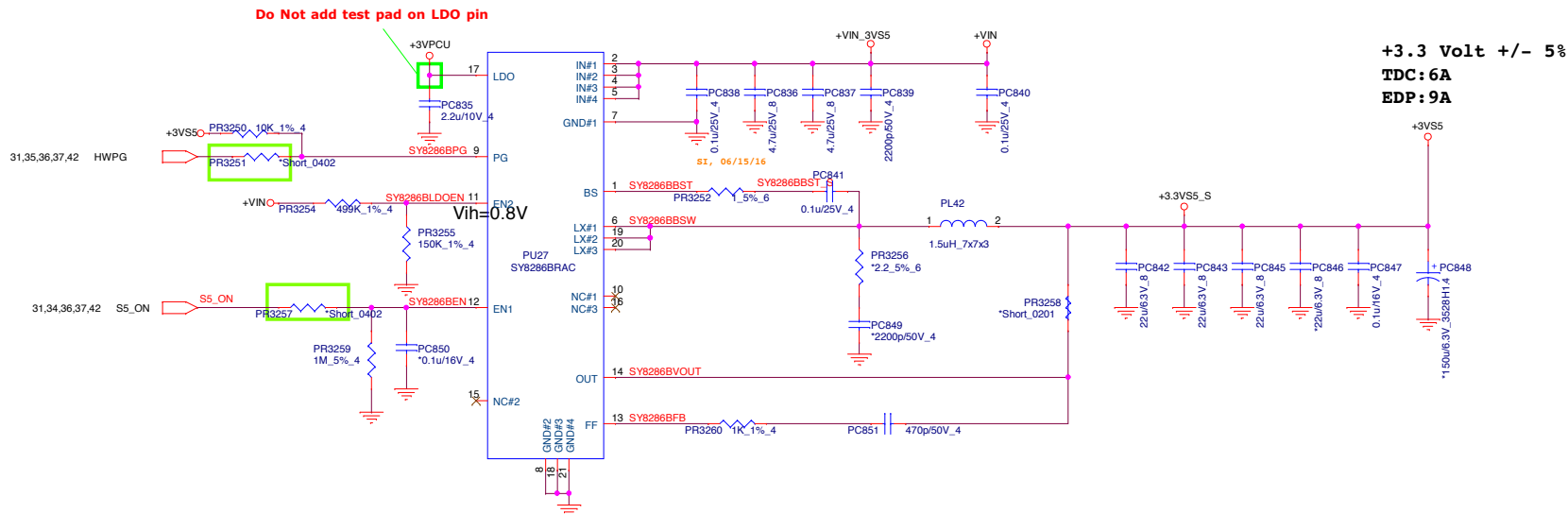
Place this cap
close to EC

Set MAX charge I to 5A

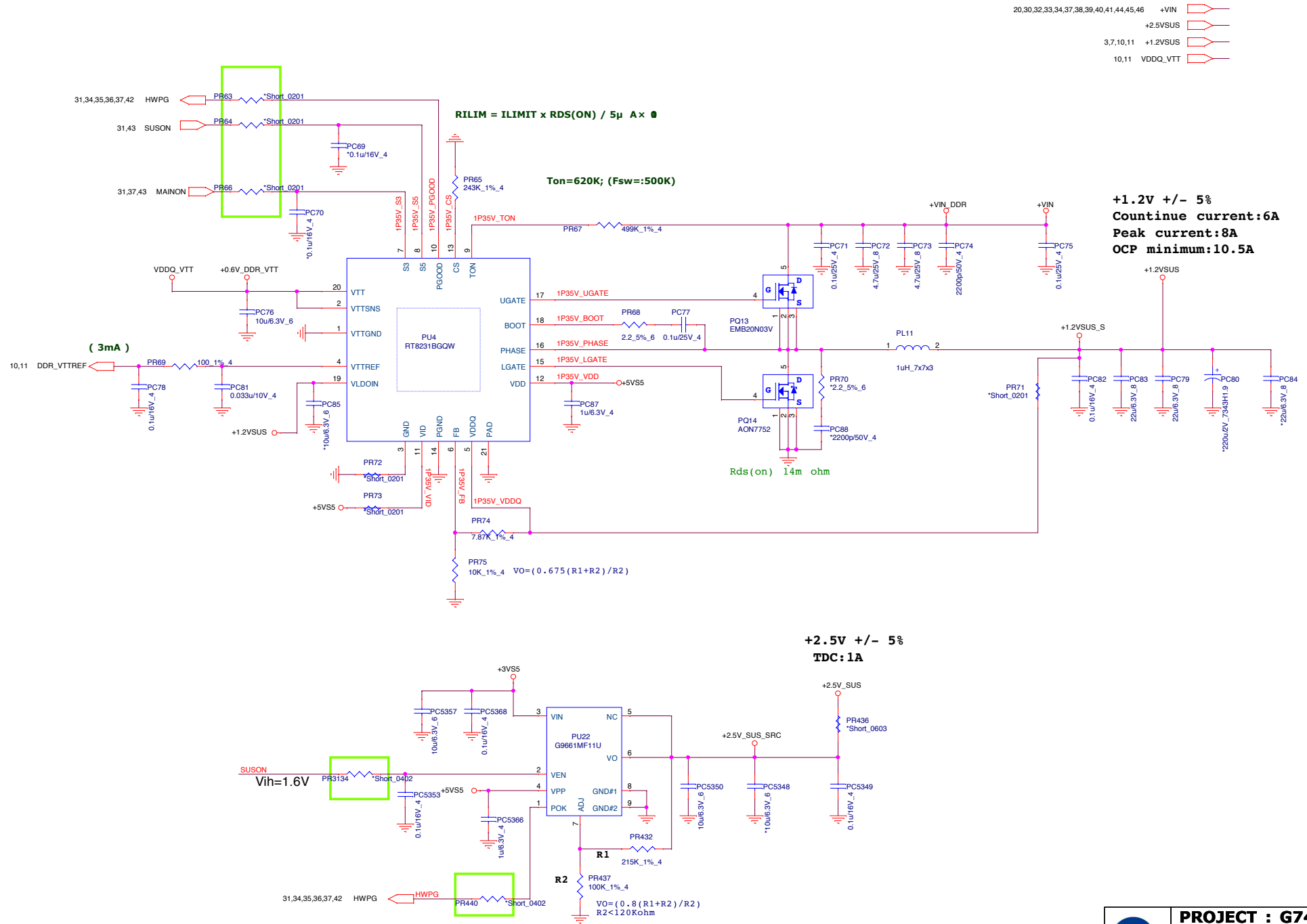


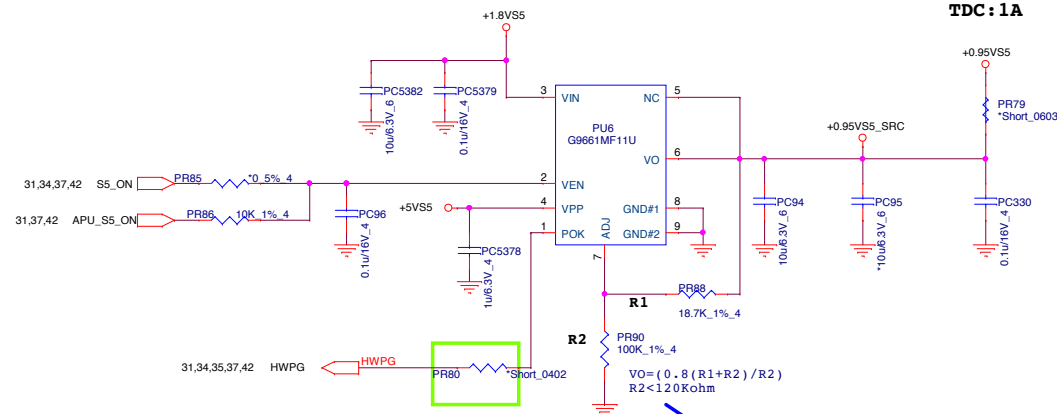
PROJECT : G74(P15-BPA)
Quanta Computer Inc.

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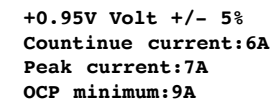
USB Charge support	Ra	Rb
Pavilion (No support)	Stuff	NA
Envy (Support)	NA	Stuff





	R1		
Stoney/Bristol	18.7K	CS31872FB19	0.95V
	31.6K	CS33162FB14	1.05V

Bristol VDDP=1.05V
Stoney VDDP=0.95V



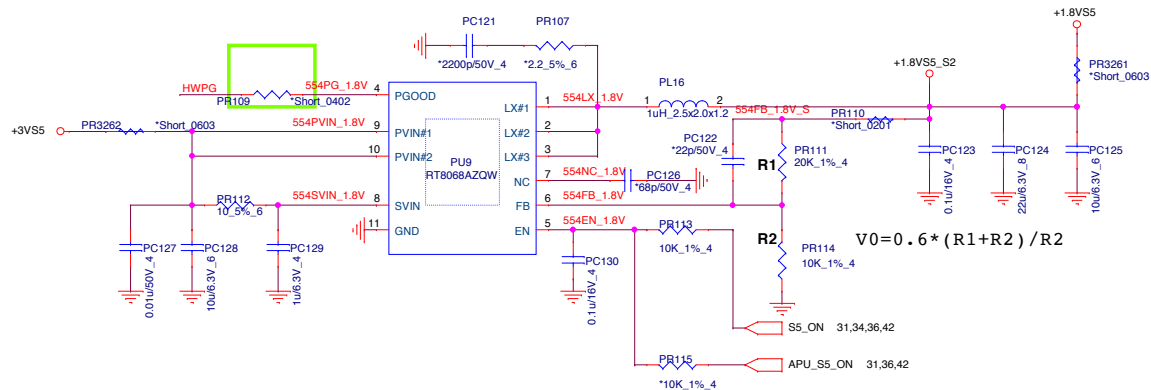
Bristol VDDP=0.95V
Stoney VDDP=0.95V

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

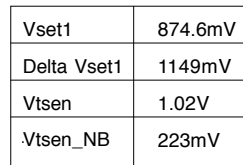
$$V_{out1} = (1 + R1/R2) * 0.8$$

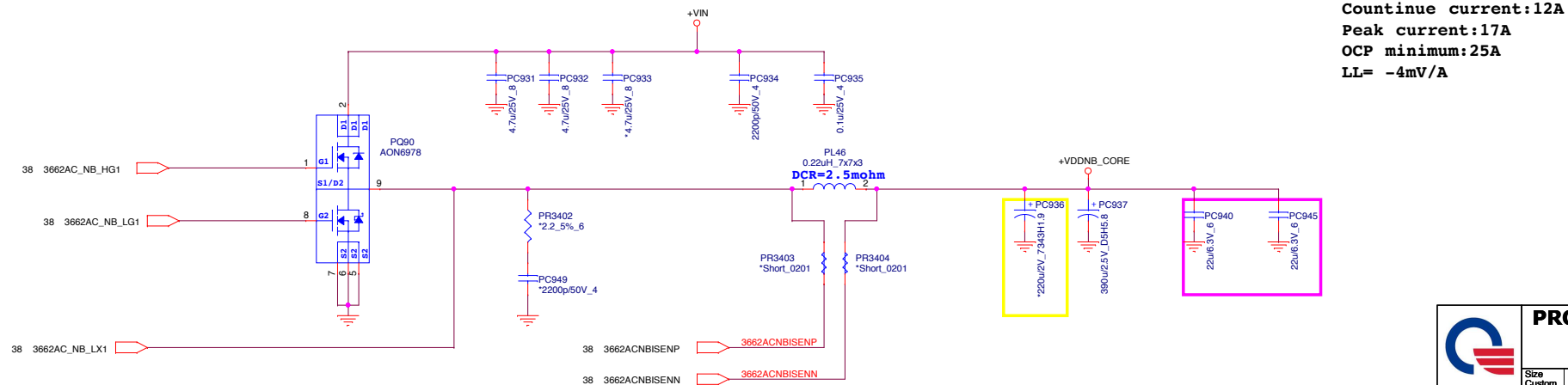
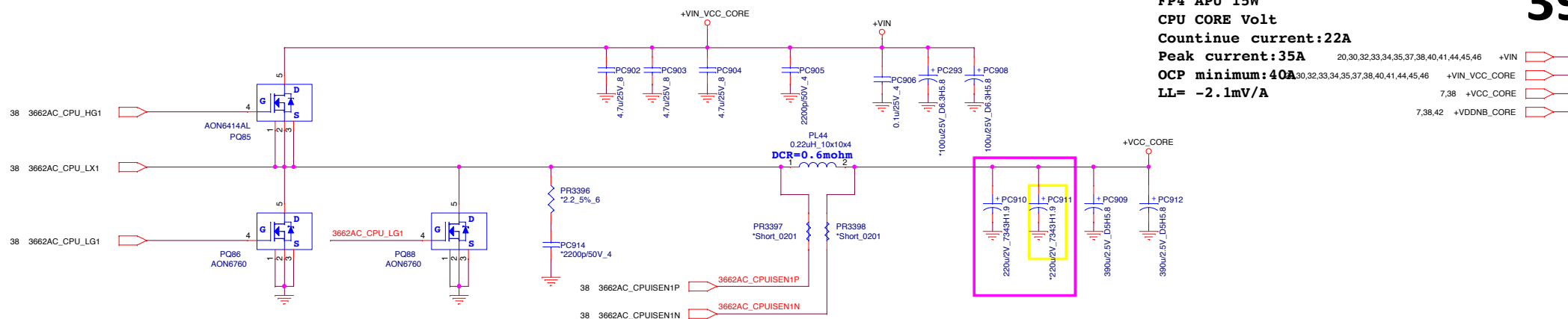
	R1		
Stoney / Bristol	1.91K	CS21912FB13	0.95V
	3.16K	CS23162FB04	1.05V

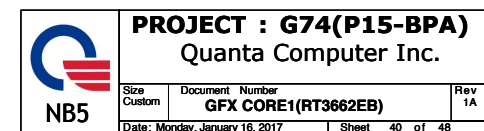
1.8VS5 +/- 3%
TDC: 3A
EDP: 4A



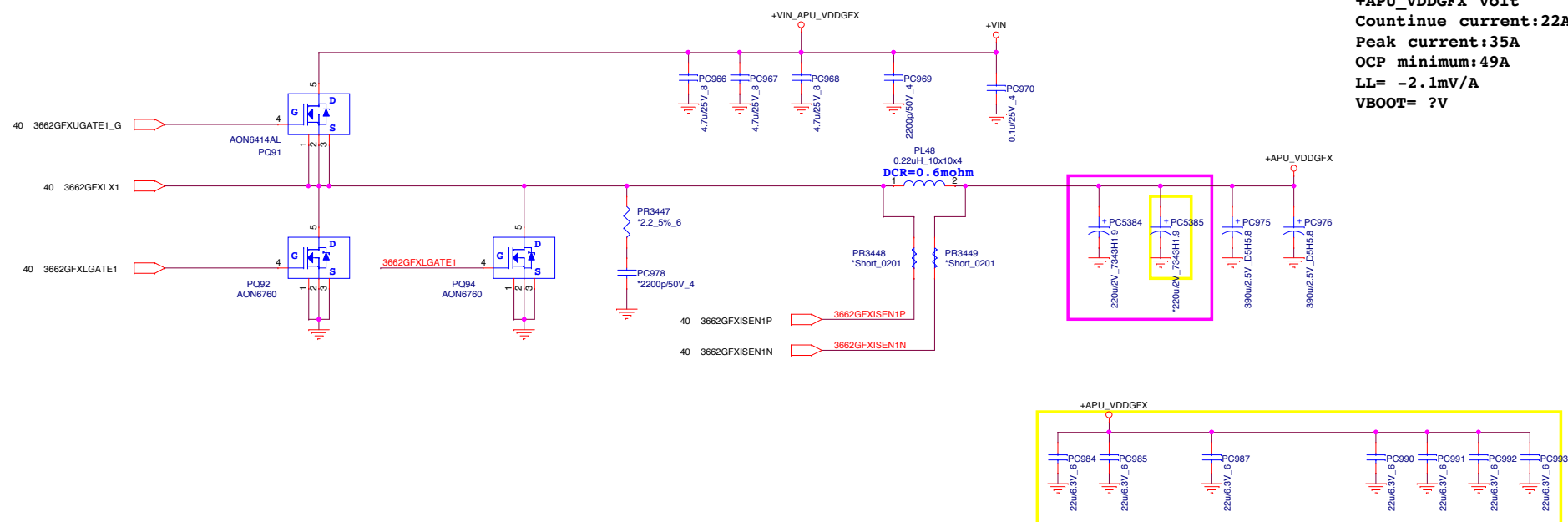
$$V_0 = 0.6 * (R_1 + R_2) / R_2$$



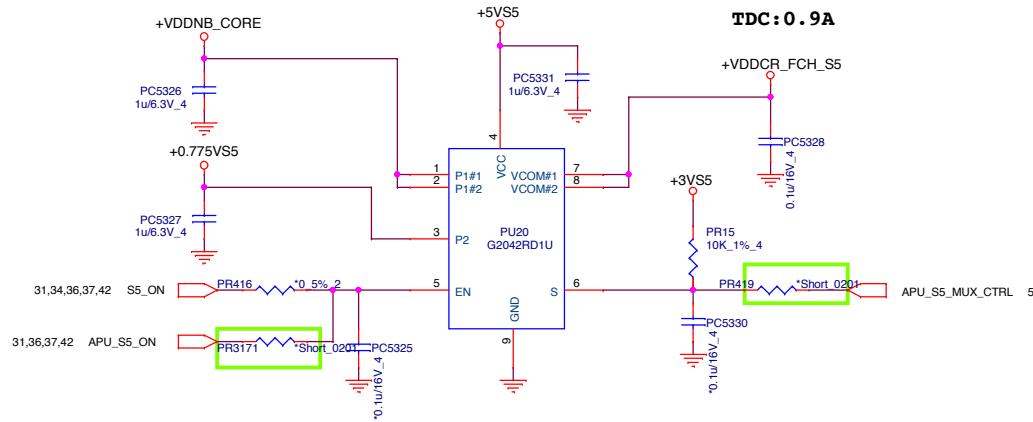




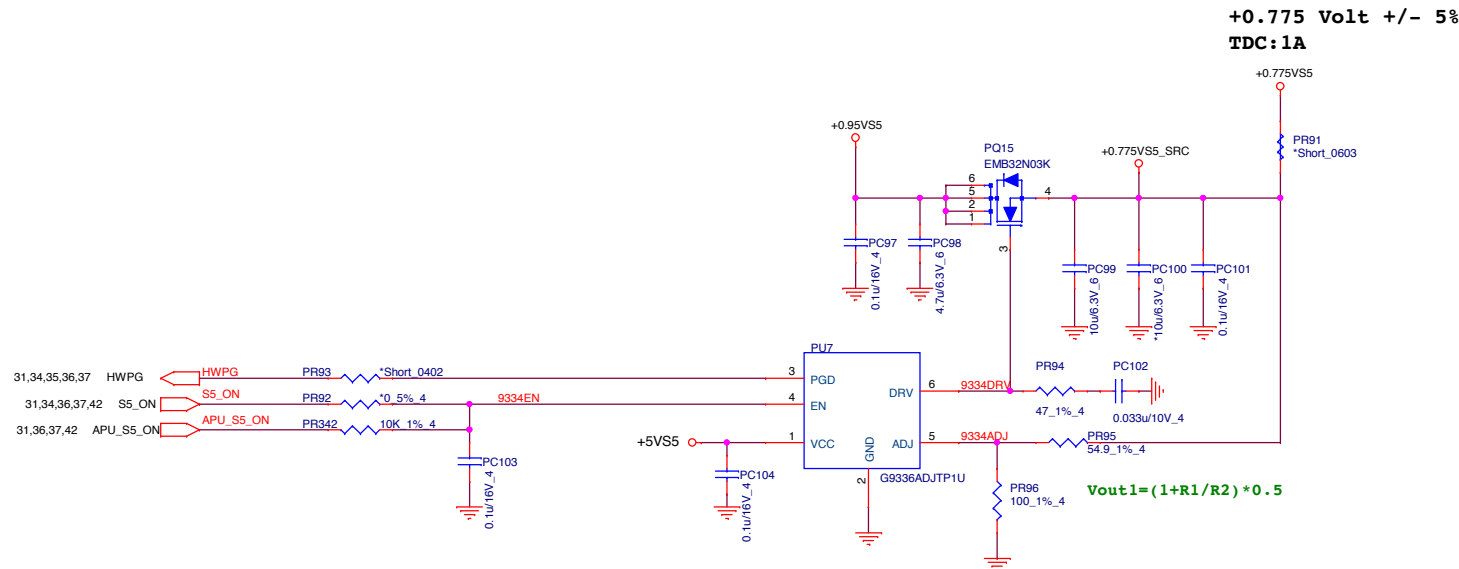
CPU	Page 40 & Page 41
Bristol	Stuff
Stonley FP4,FT4	Unstuff



```
+APU_VDDGFX Volt
Continue current:22A
Peak current:35A
OCP minimum:49A
LL= -2.1mV/A
VBOOT= ?V
```

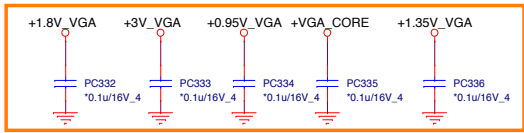


EN	SEL	VIN1	Vo
0	X	0.775V~1.2V	0V
1	0	<0.775V	0.775V
1	0	>0.775V	VDDNB
1	1	0.775V~1.2V	VDDNB

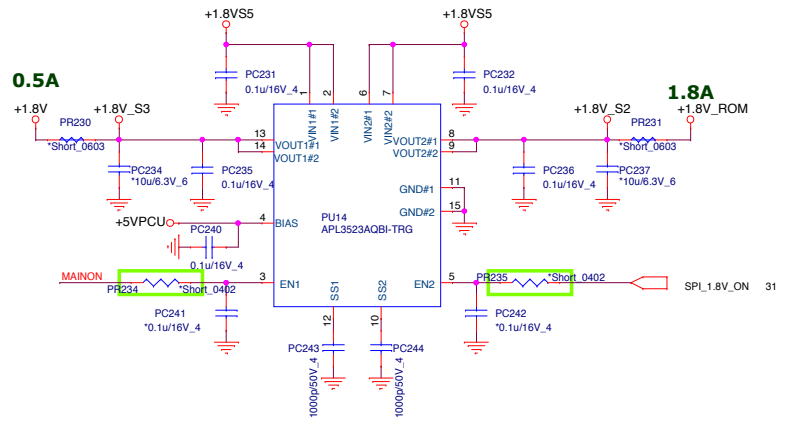
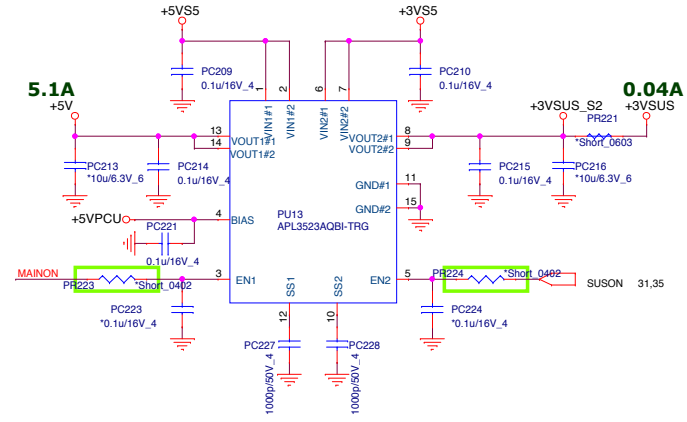
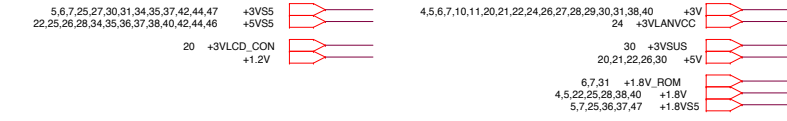
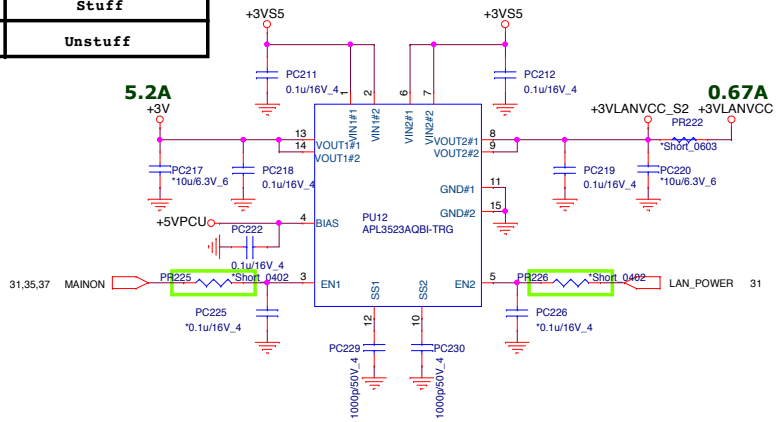


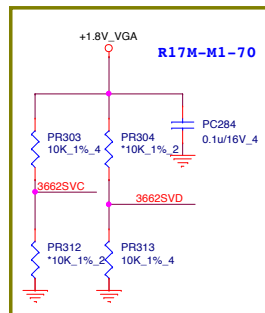
PROJECT : G74(P15-BPA)
Quanta Computer Inc.

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UMA only	Stuff
discrete	Unstuff

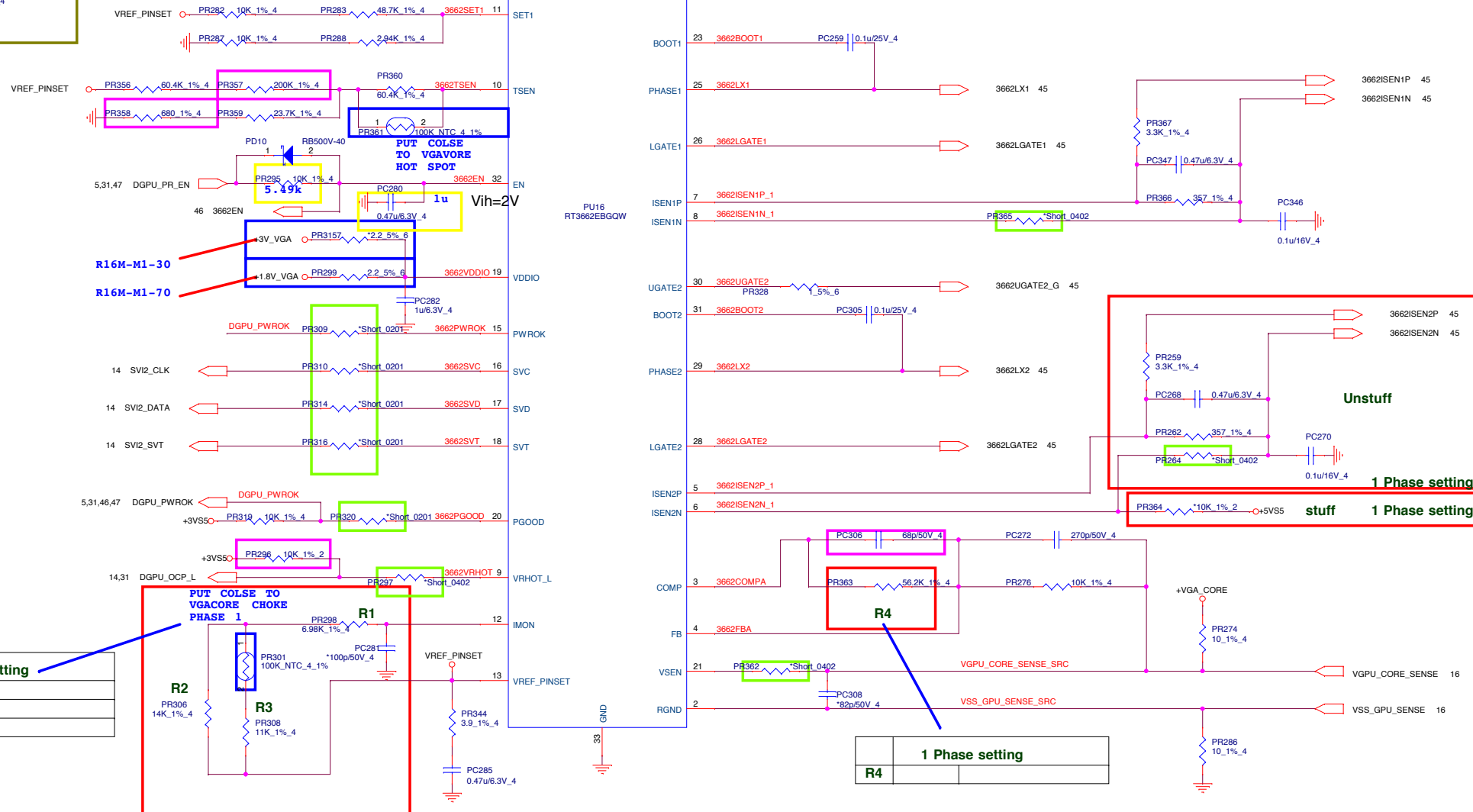




VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

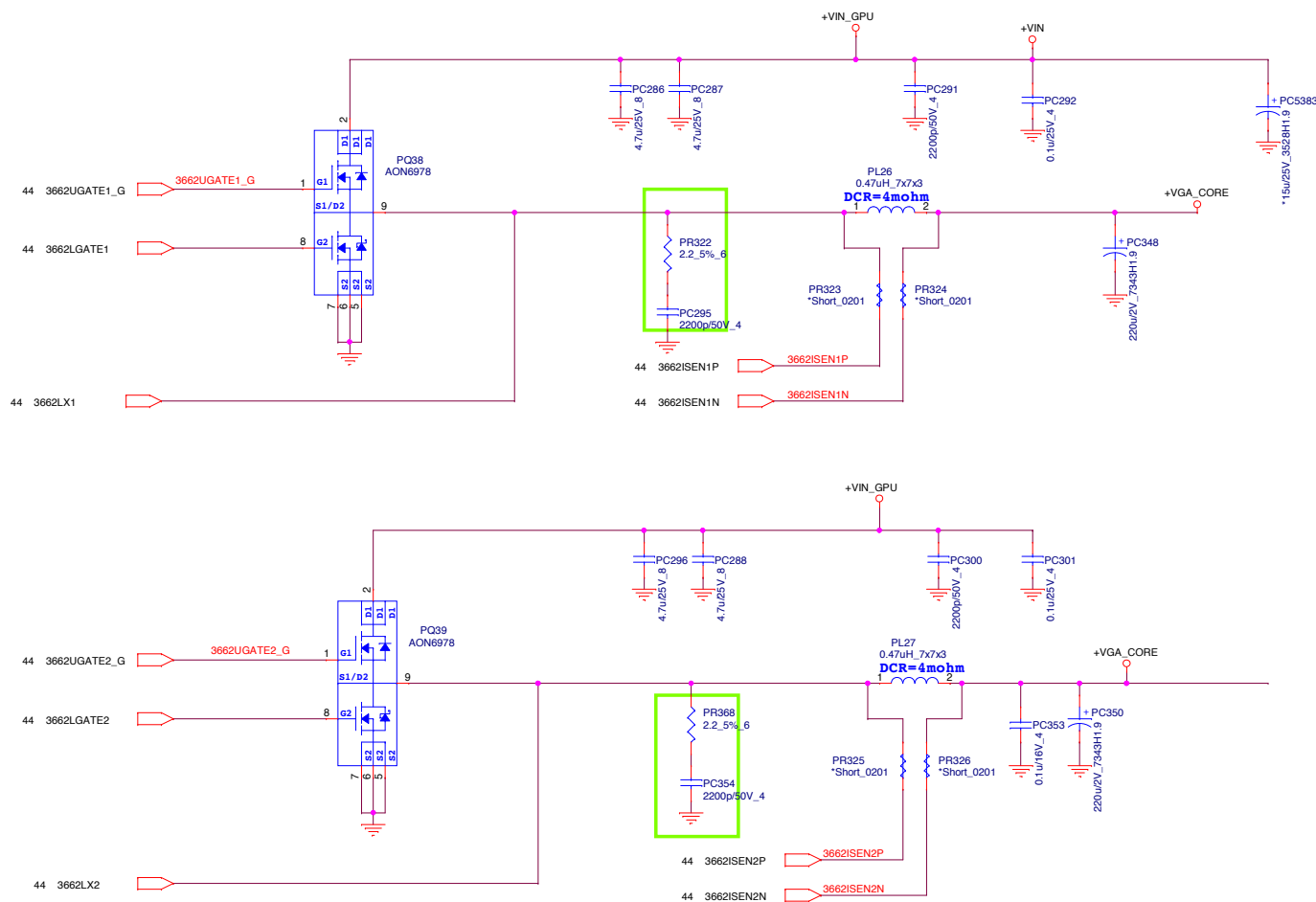
20,30,32,33,34,35,37,38,39,40,41,45,46	+VIN_GPU
22,25,26,28,34,35,36,37,38,40,42,43,46	+5VS5
16,43,45	+VGA_CORE
13,14,16,43,47	+1.8V_VGA



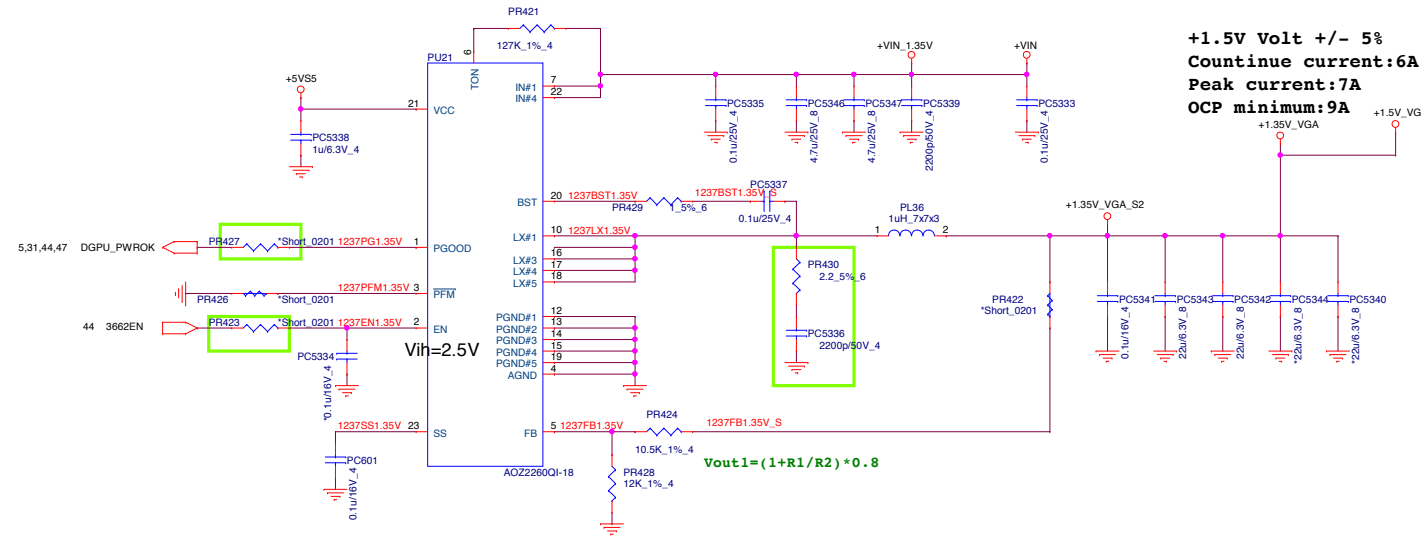
	1 Phase setting
R1	
R2	
R3	

20,30,32,33,34,35,37,38,39,40,41,44,46 +VIN
 20,30,32,33,34,35,37,38,39,40,41,44,46 +VIN_GPU
 16,43,44 +VGA_CORE

VGACORE (R17M-M1-70 25W/38W(1ms))
Countinue current:28A
Peak current=38A (1ms)
PHOCP_TDC=40A (soft-start only)
OCPI_SPIKE=55A(1ms)
Boot VID=0.9V
LL=1m V/A



20,30,32,33,34,35,37,38,39,40,41,44,45 +VIN
22,25,26,28,34,35,36,37,38,40,42,43,44 +5VSS
16,17,18,19,43 +1.5V_VGA

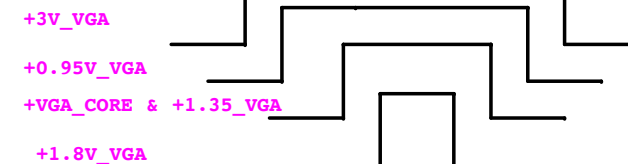
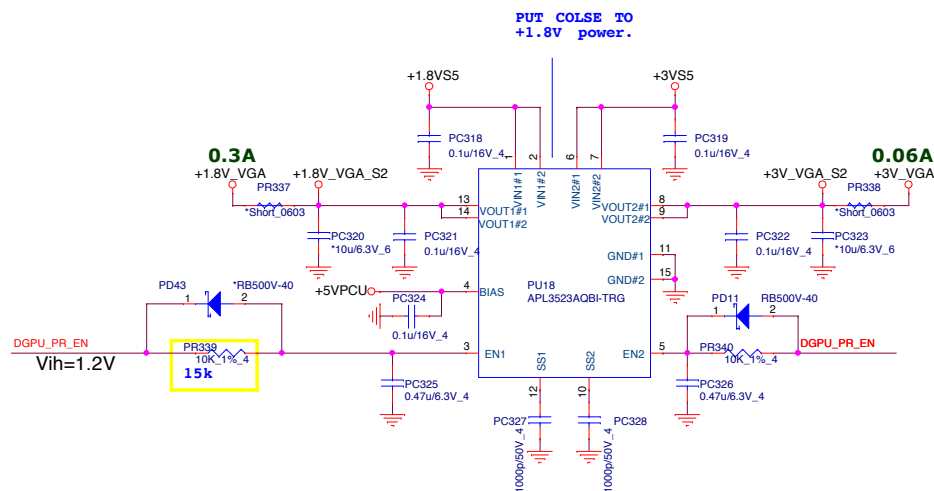
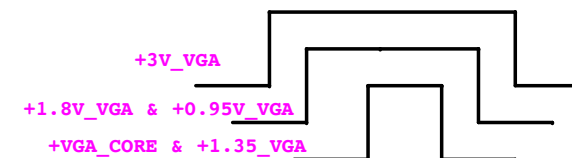
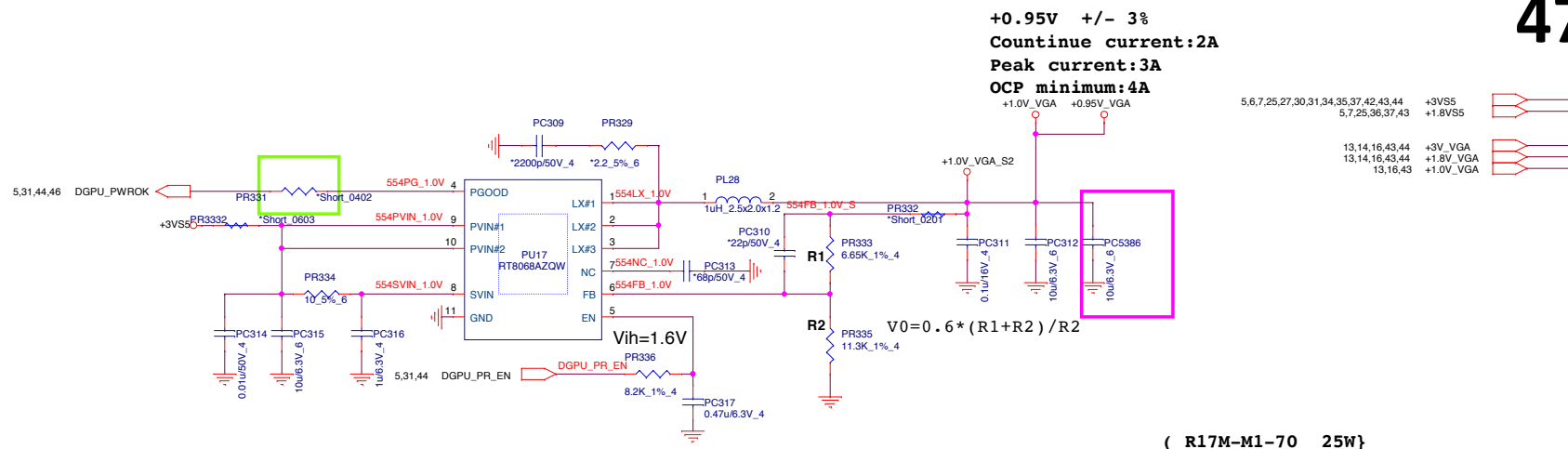


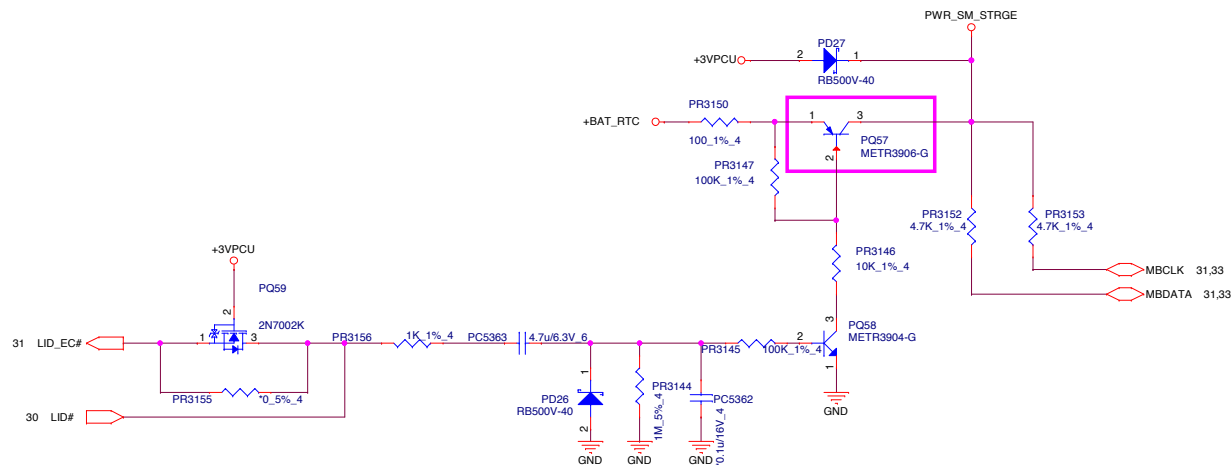
Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



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